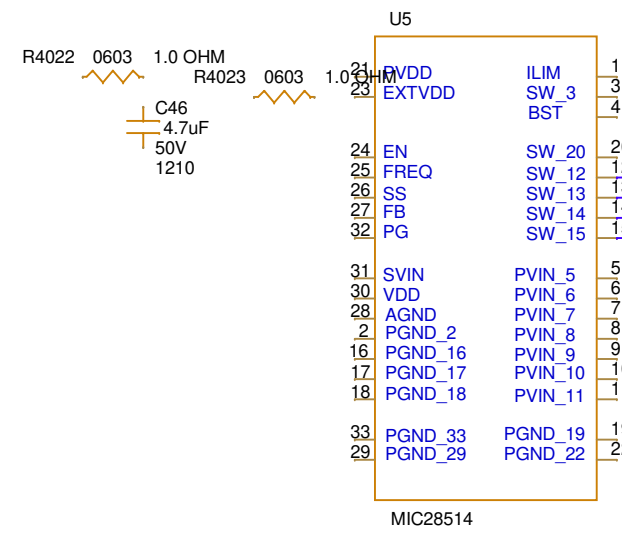
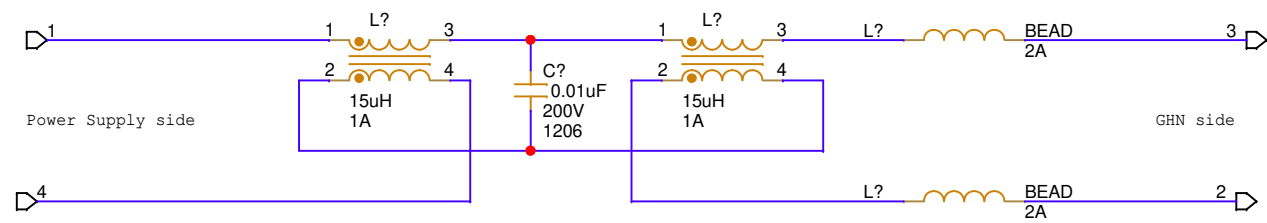


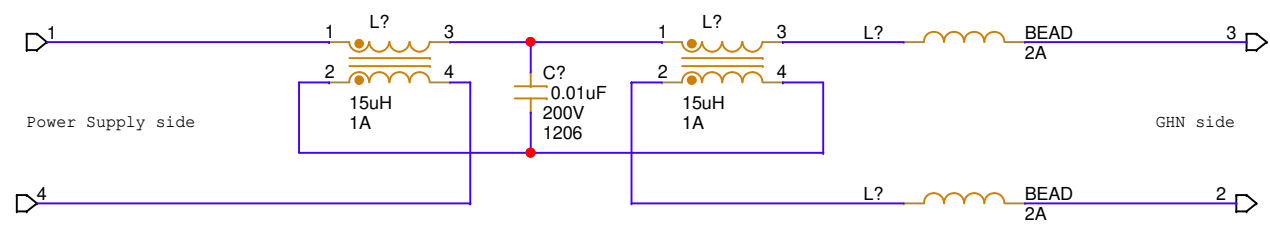
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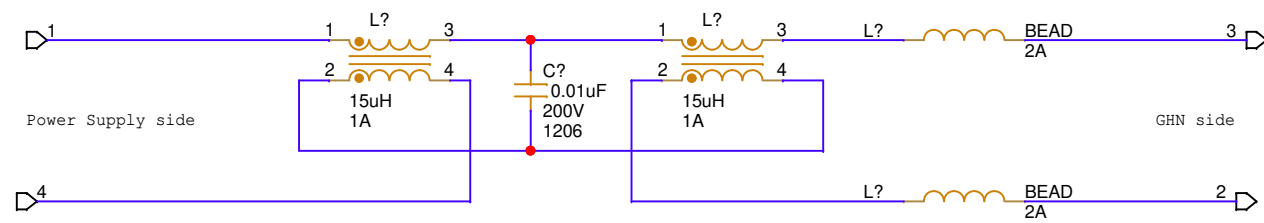
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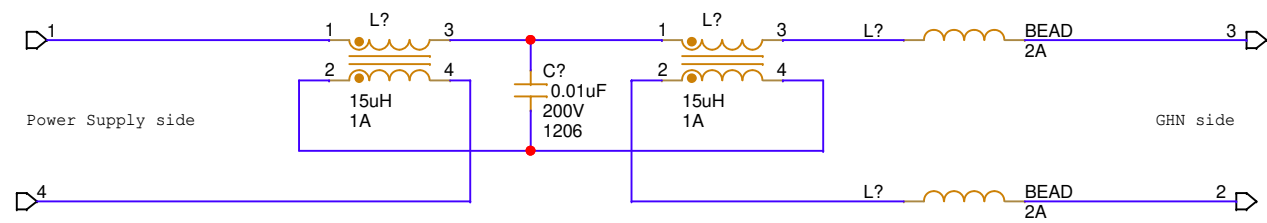
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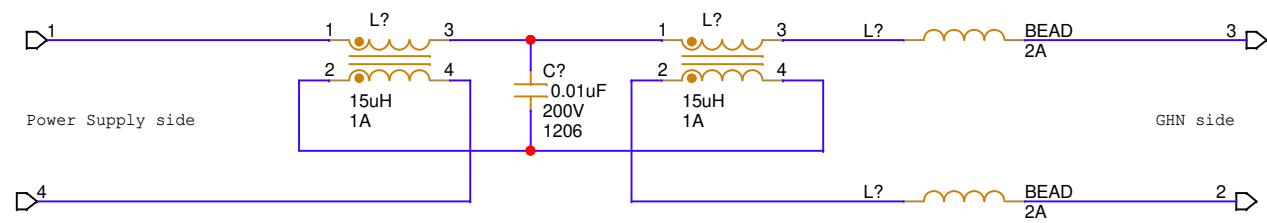
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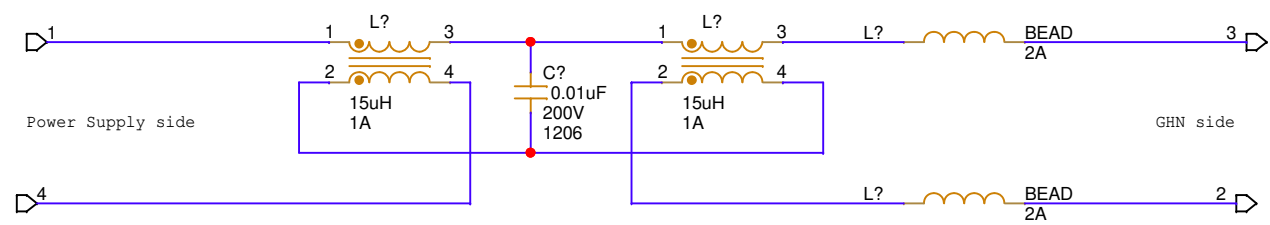
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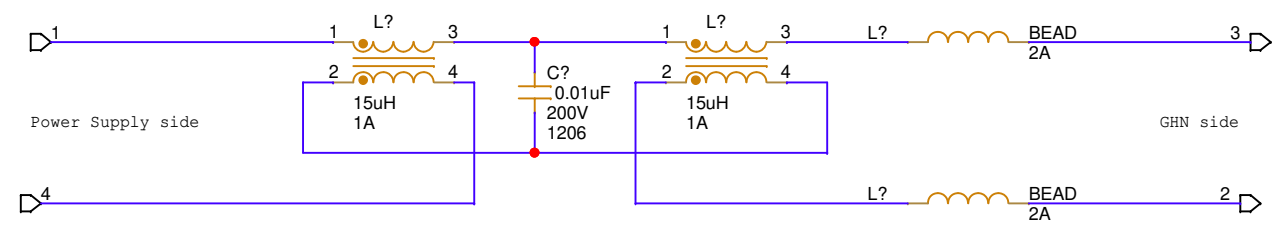


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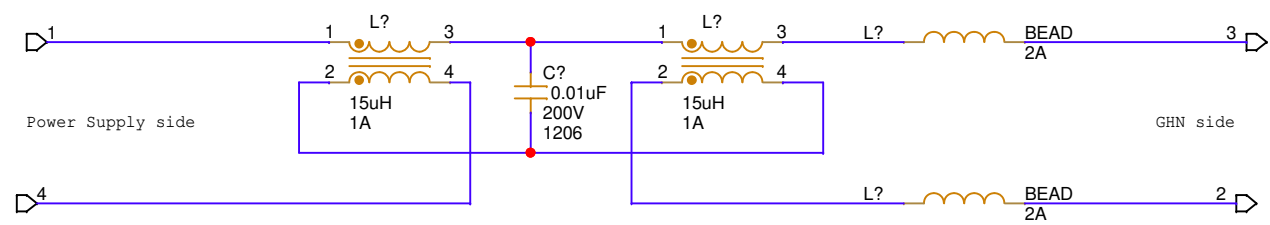


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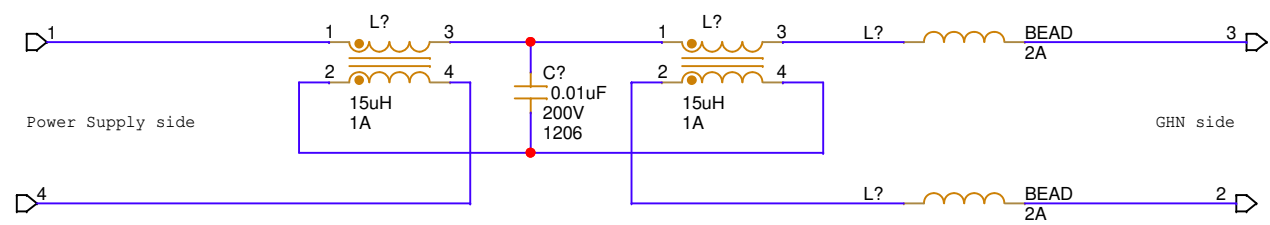




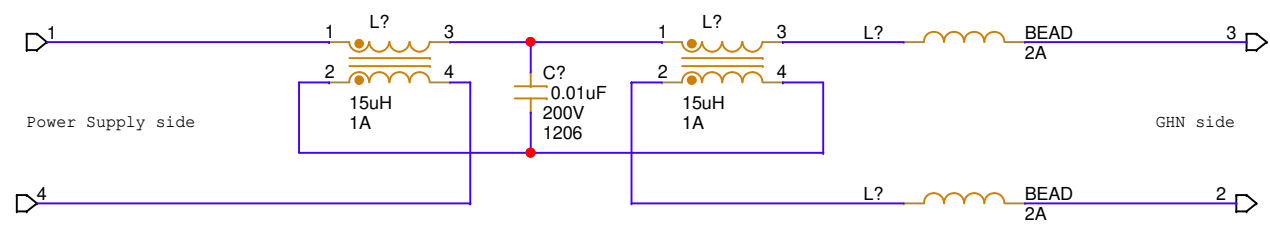
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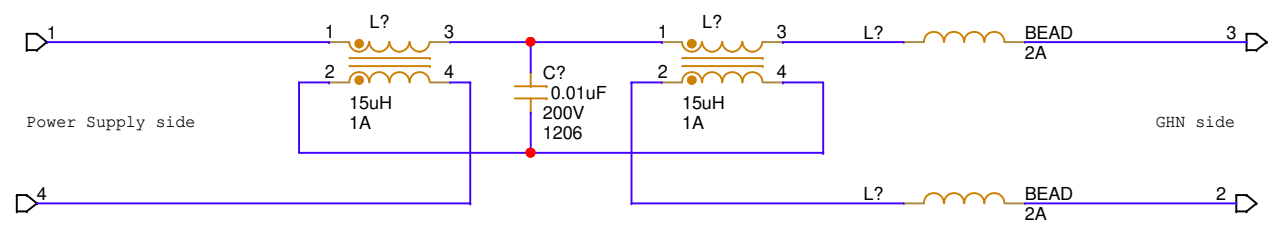
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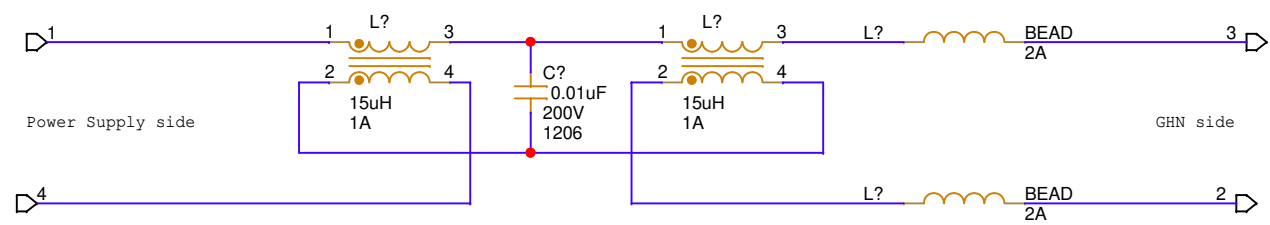
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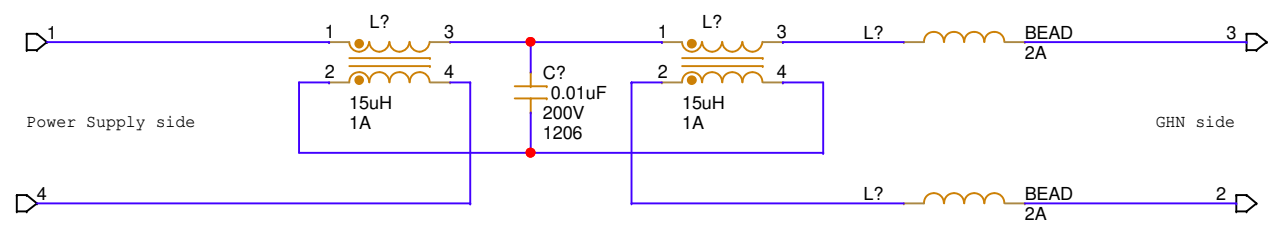
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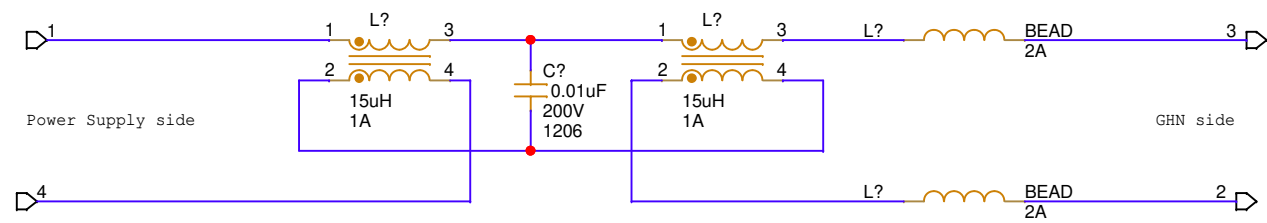
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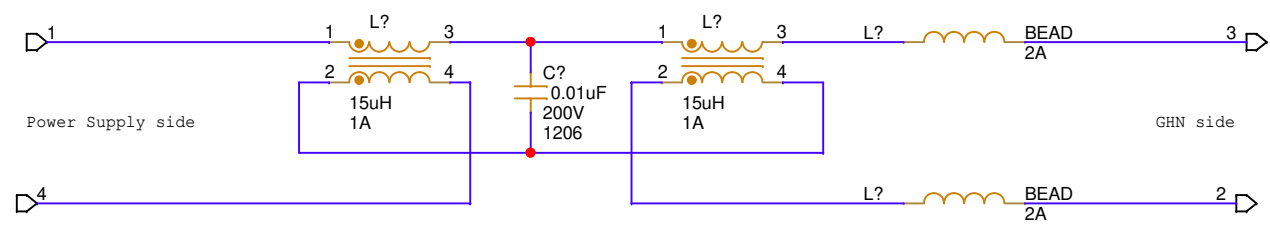


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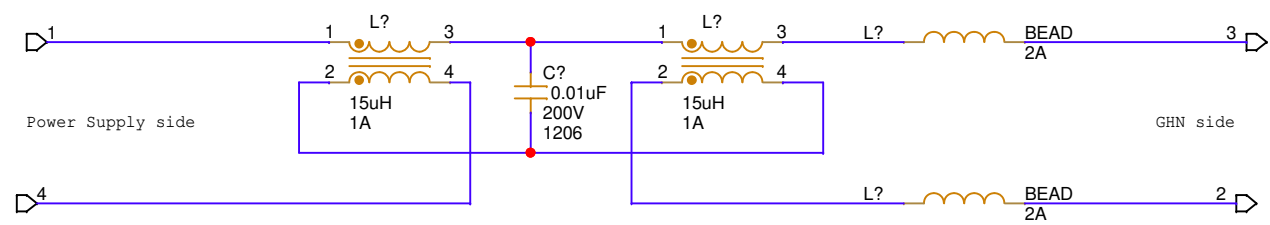


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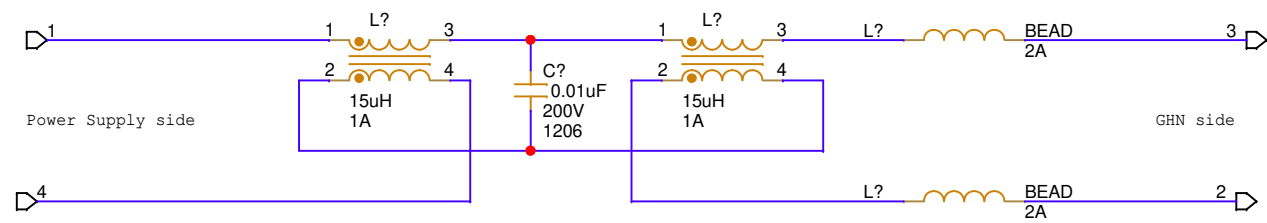




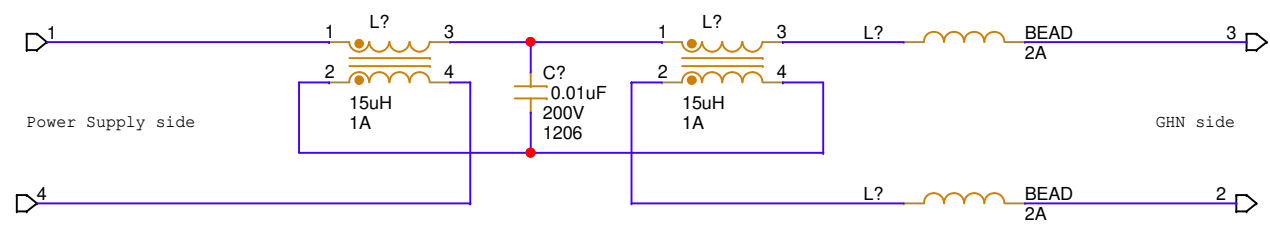
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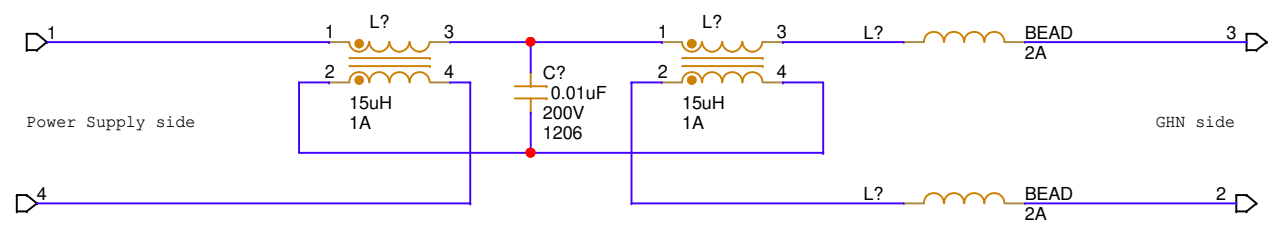
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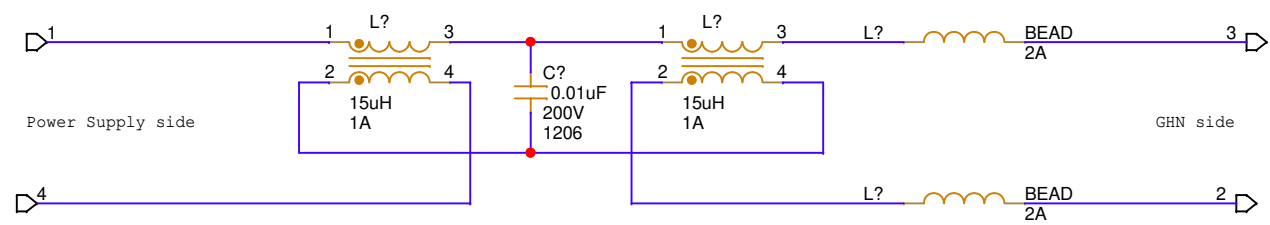
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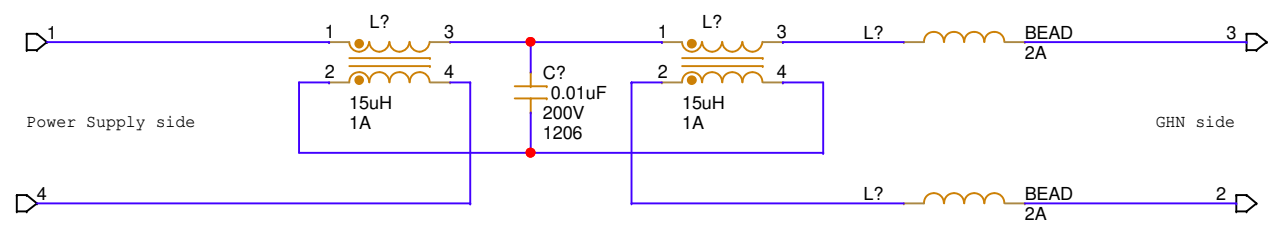
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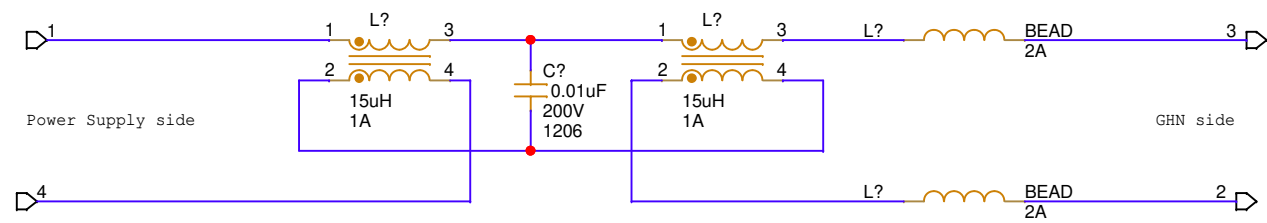
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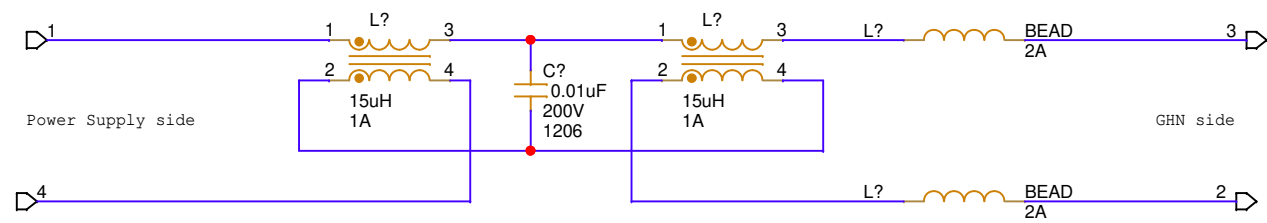


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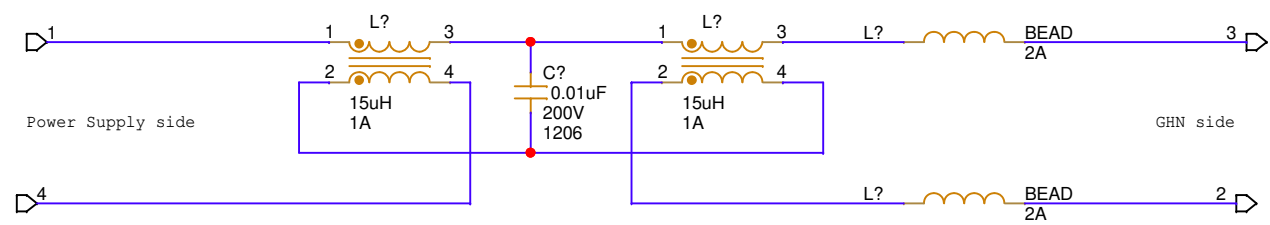


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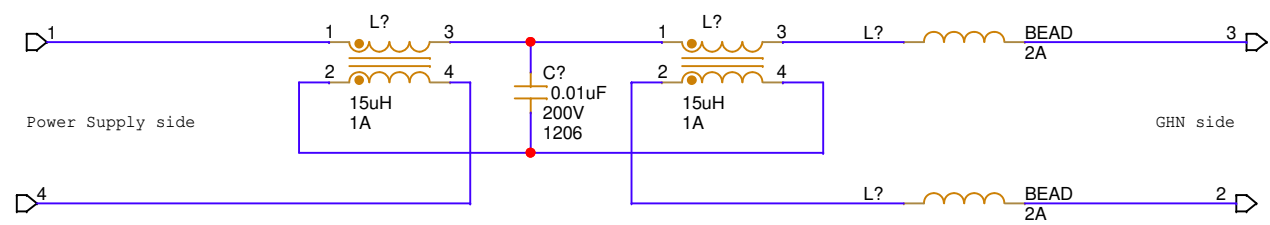




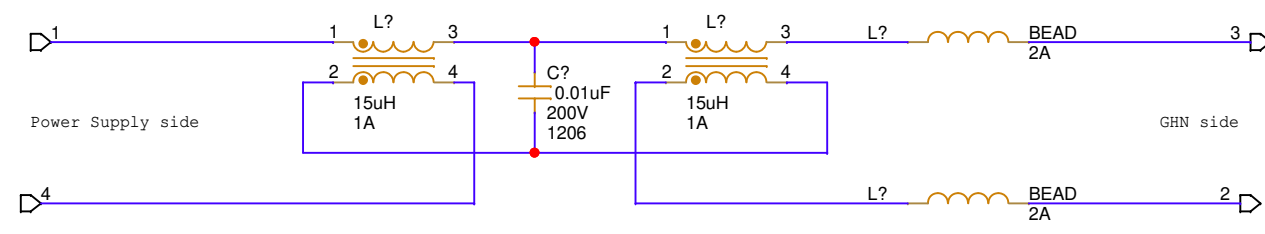
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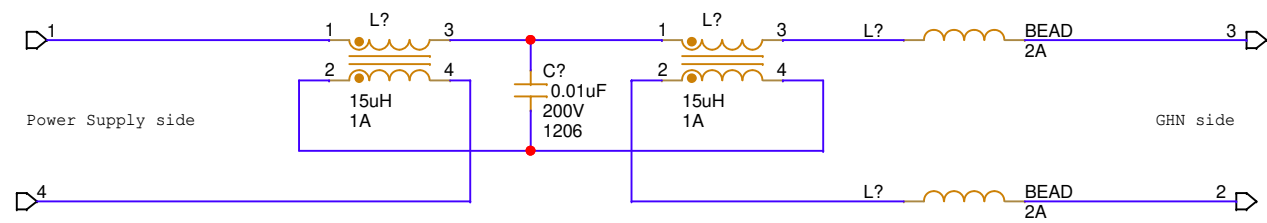
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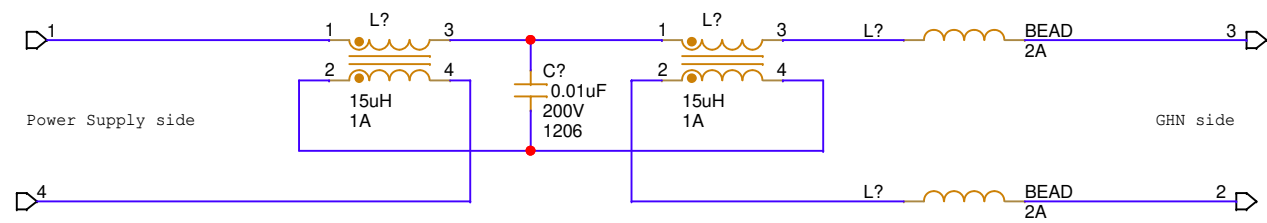
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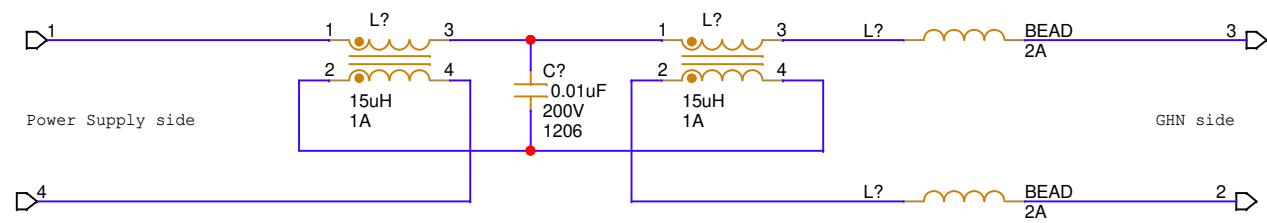
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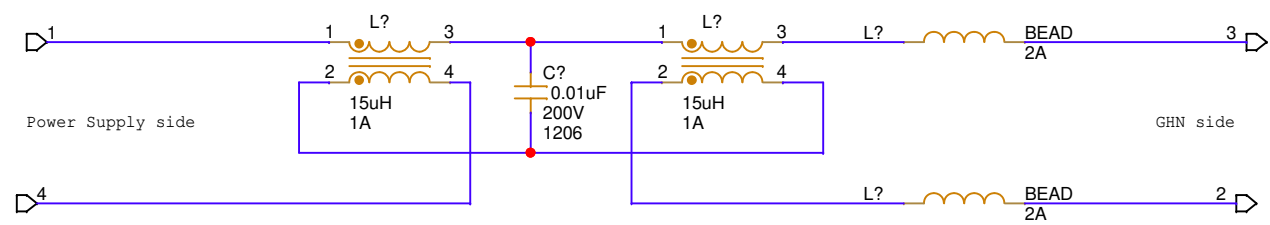
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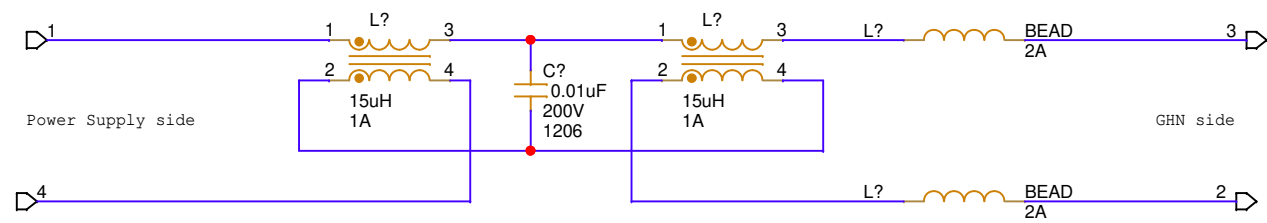


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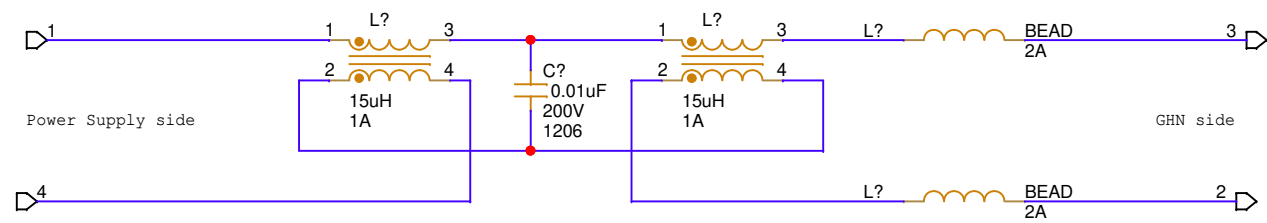


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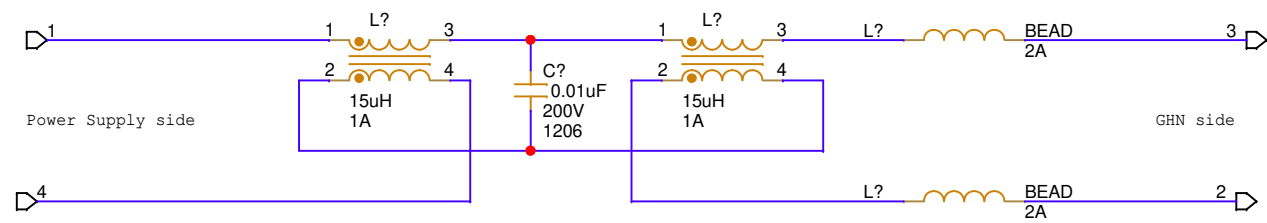




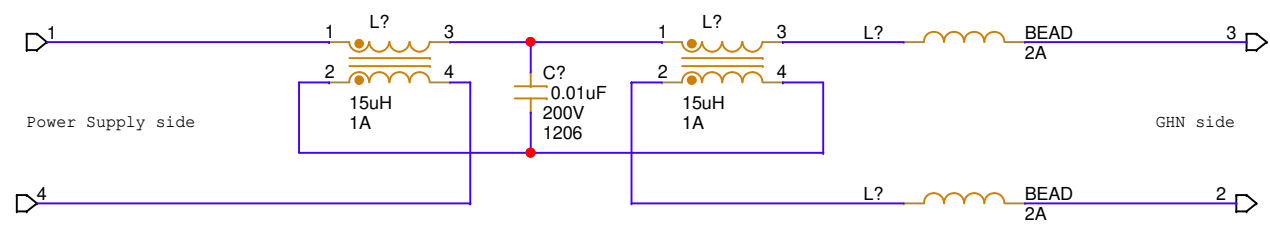
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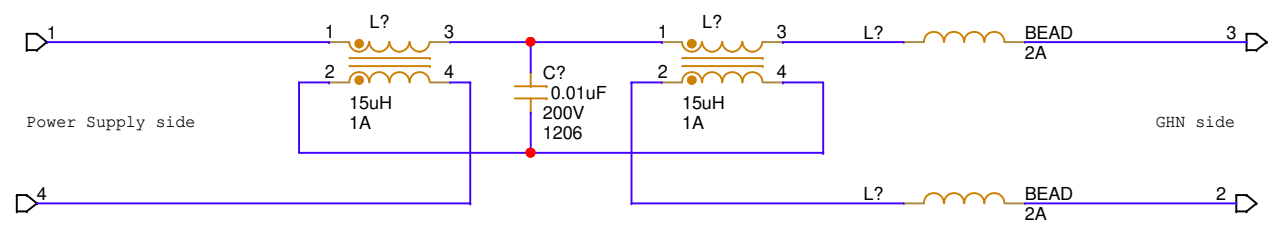
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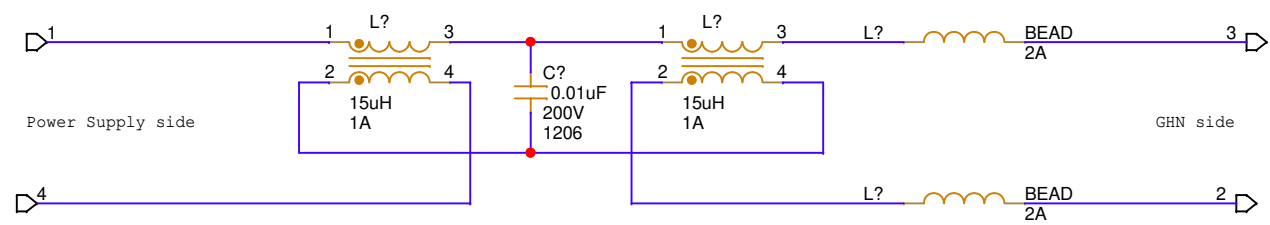
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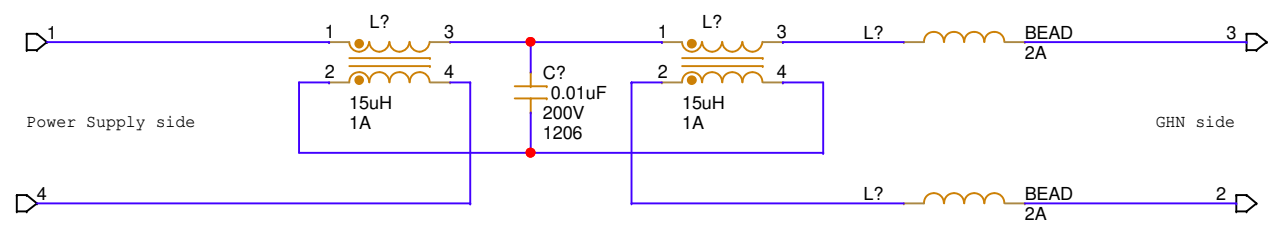
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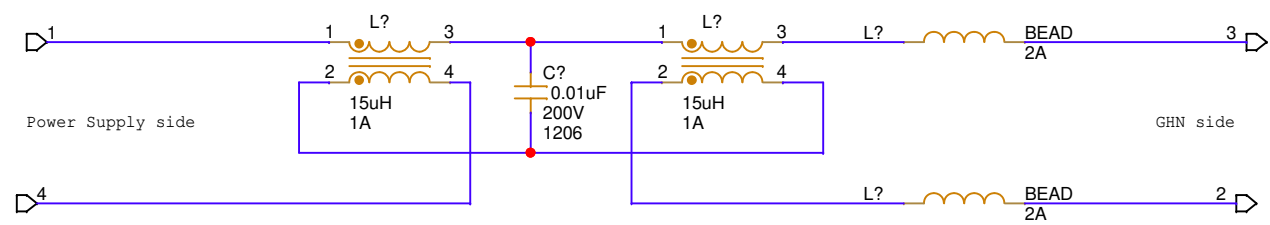
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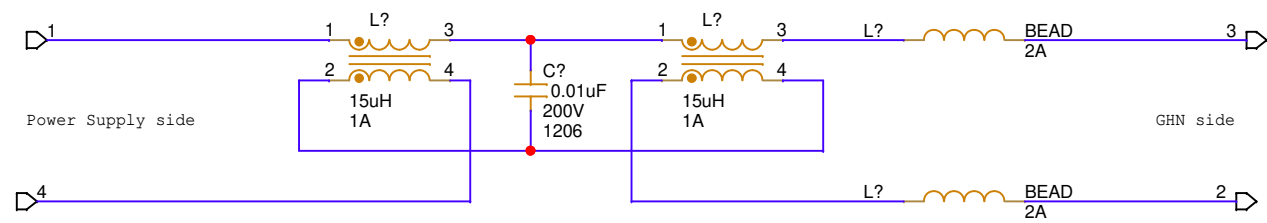


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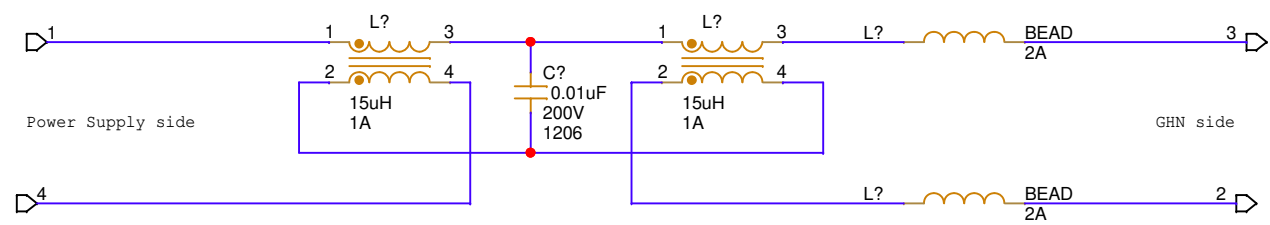


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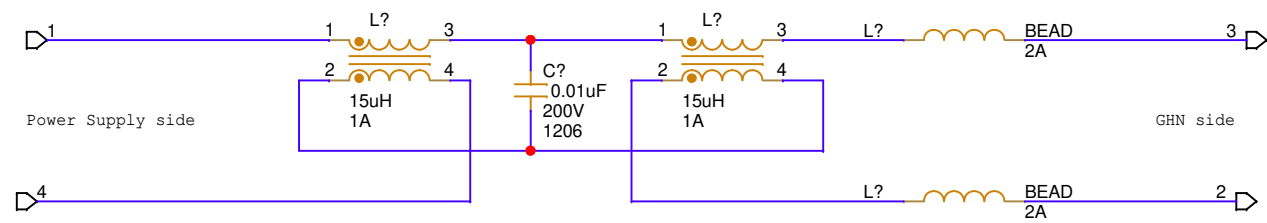




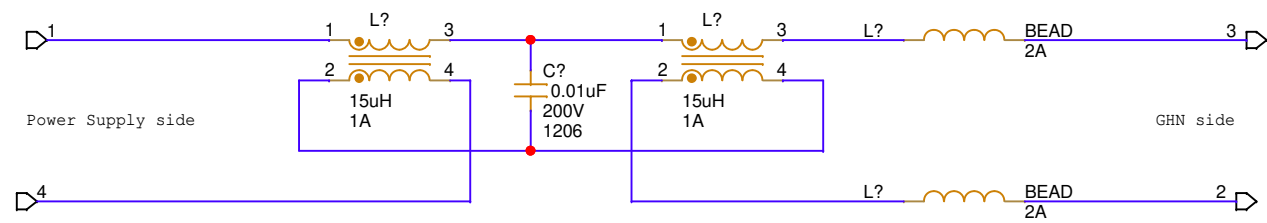
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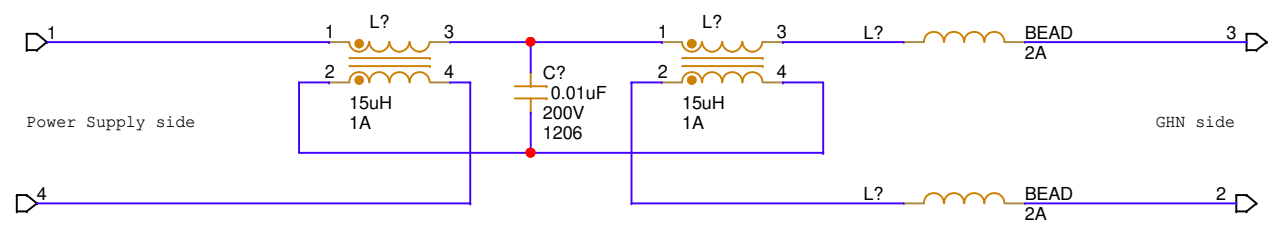
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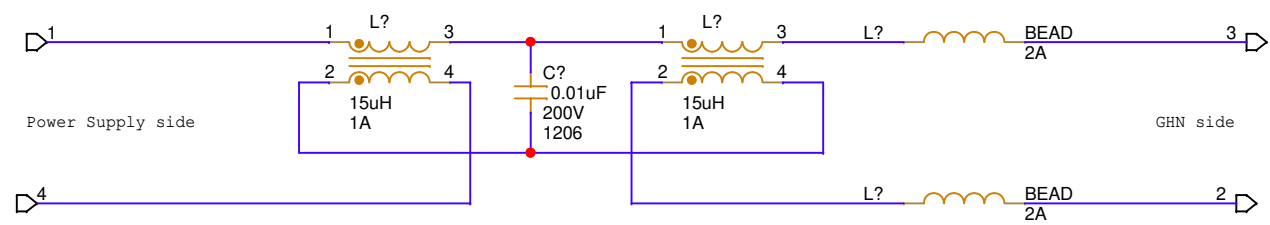
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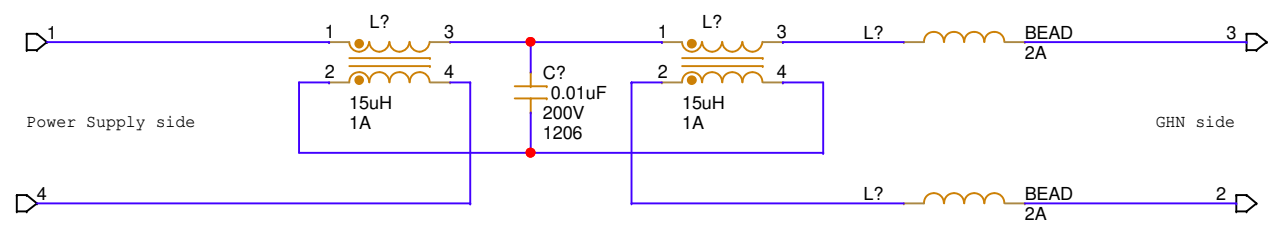
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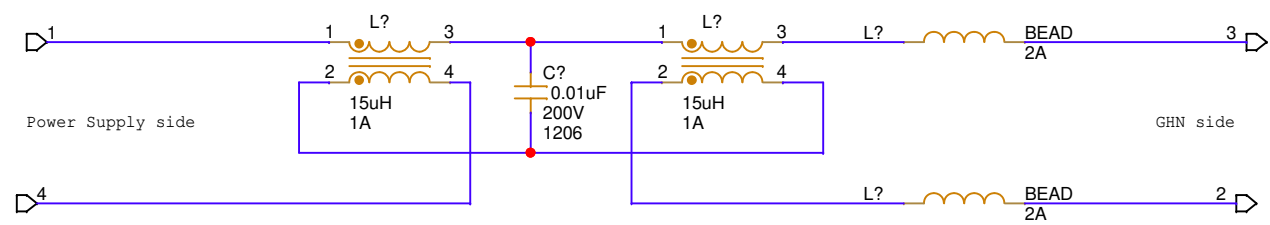
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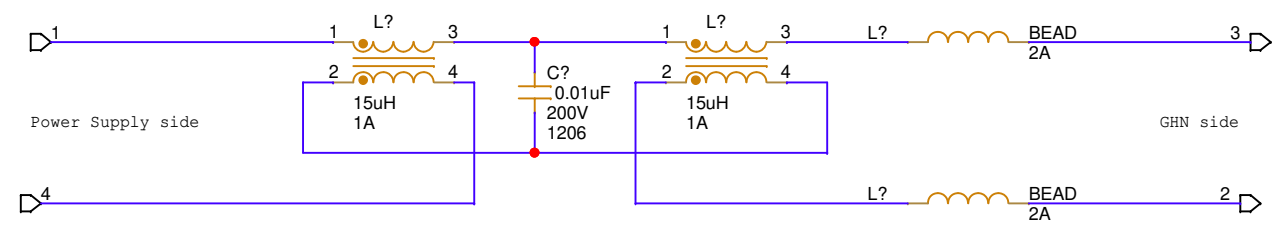


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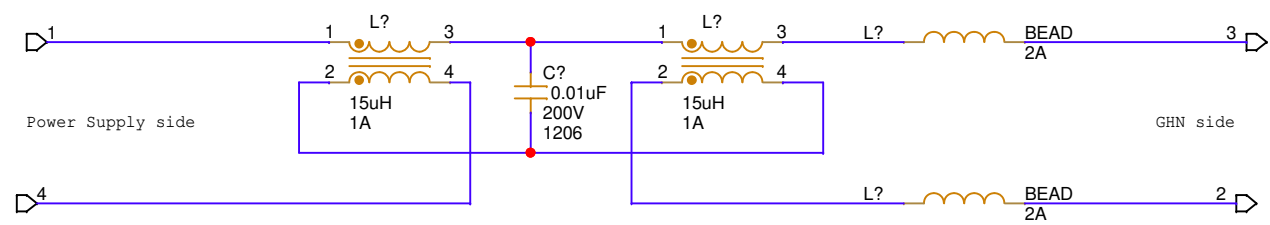


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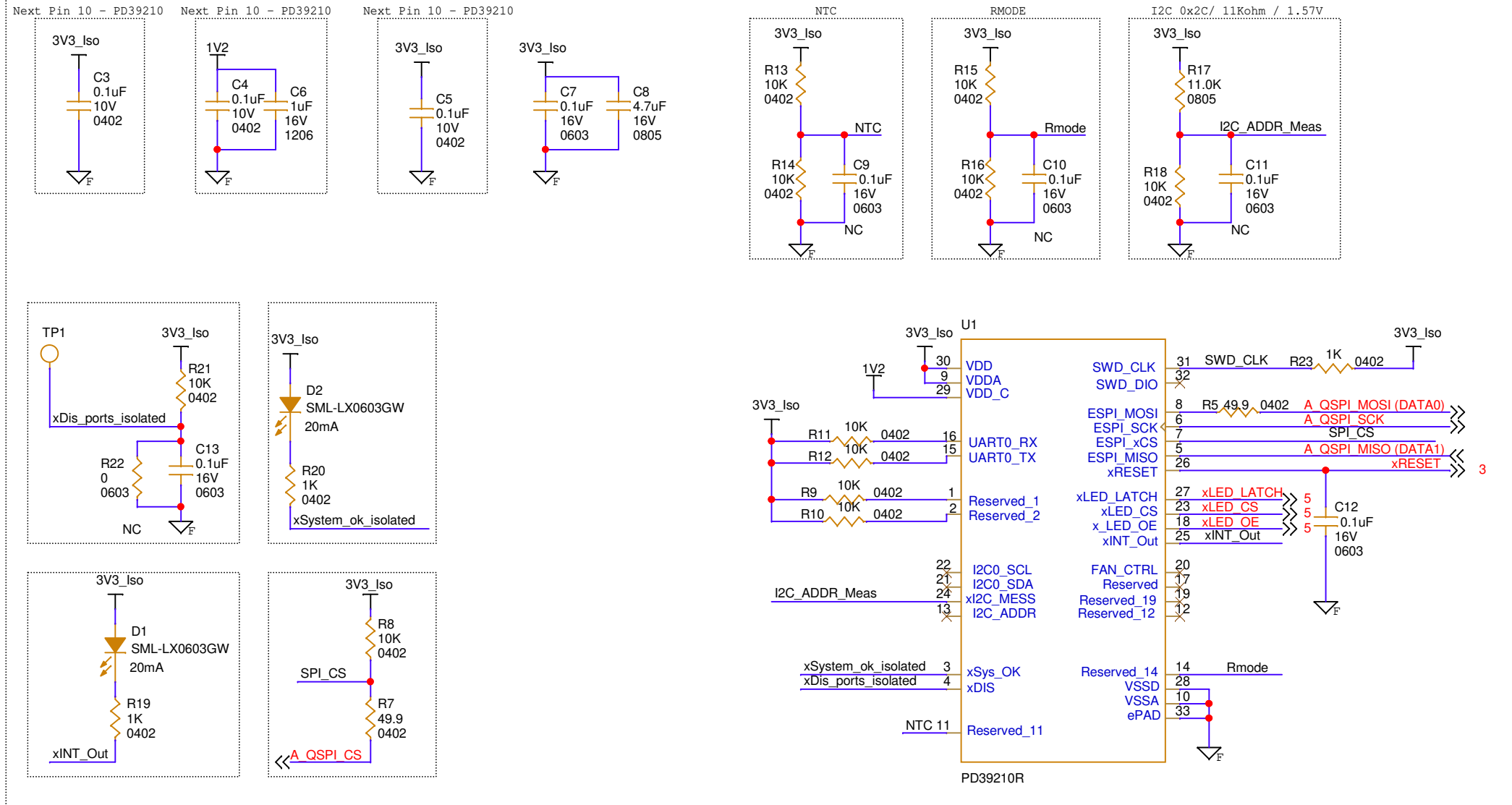


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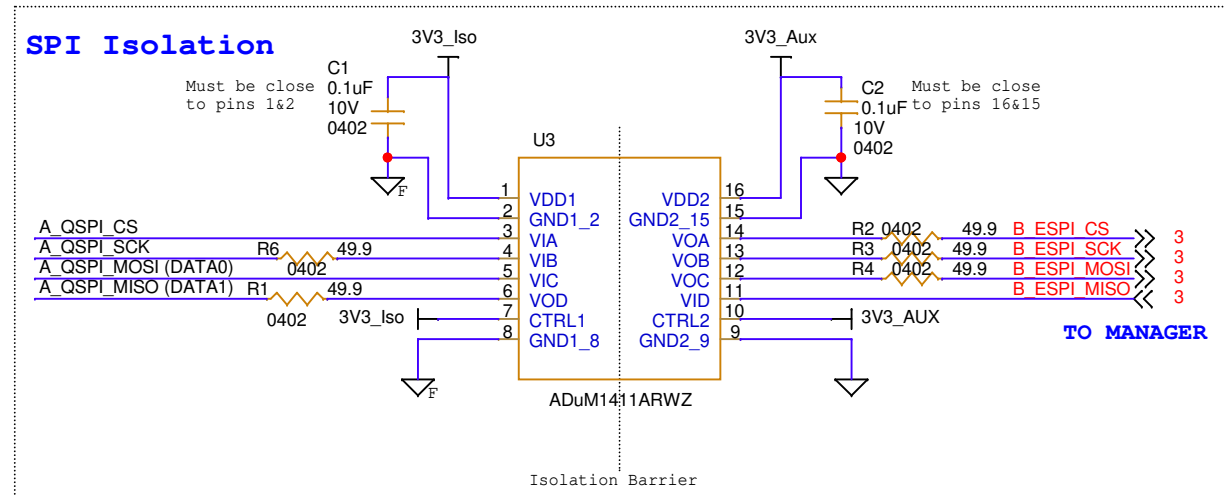


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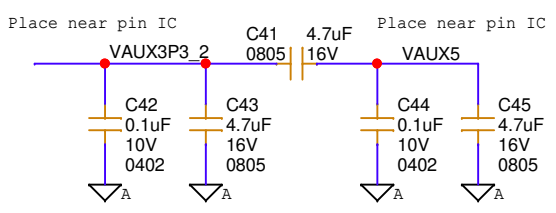
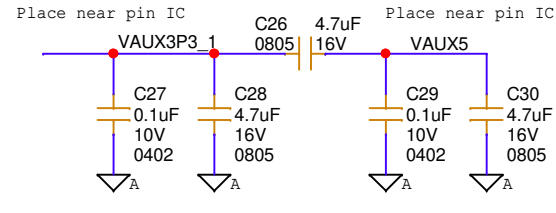
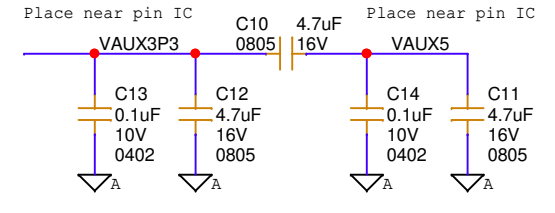
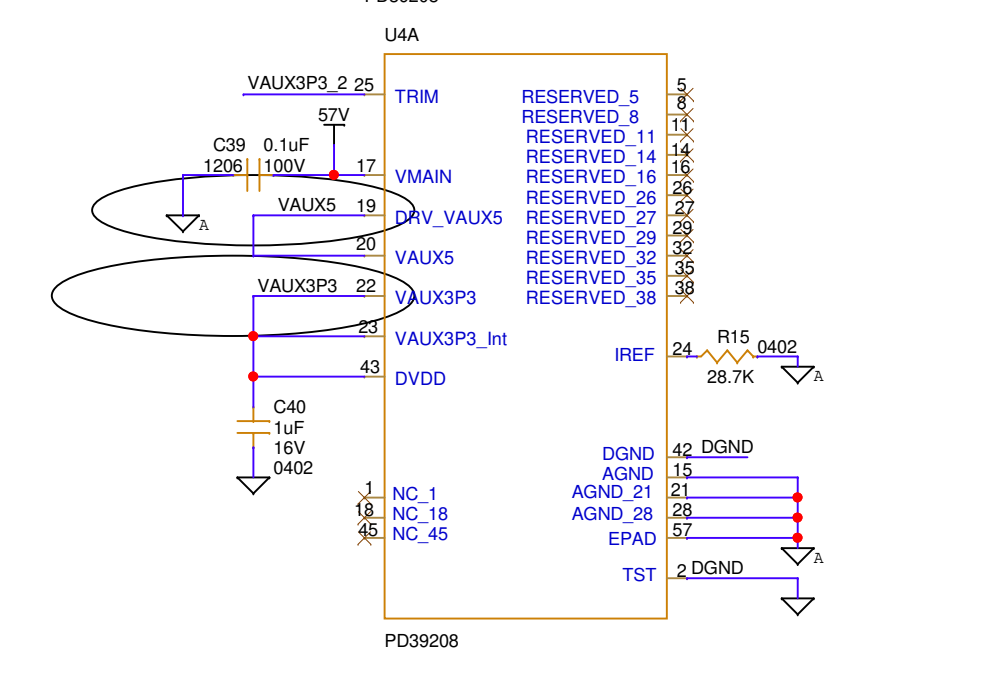
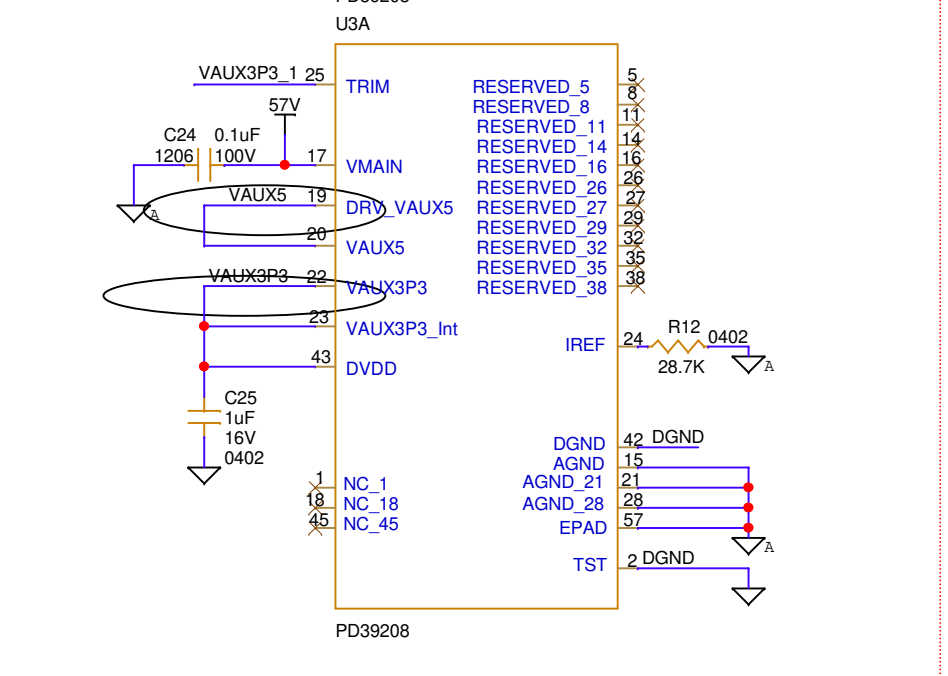
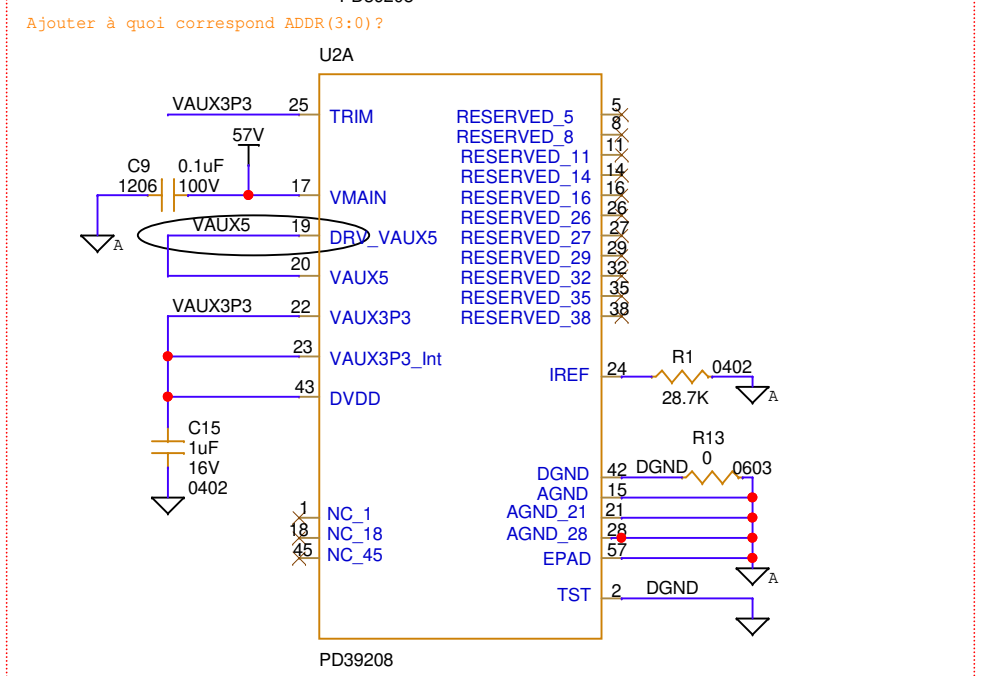
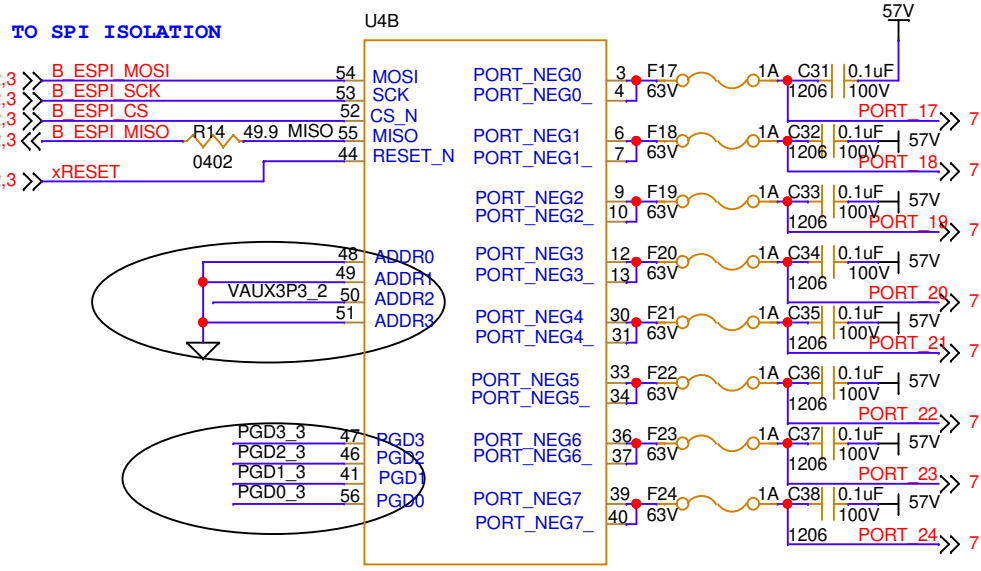
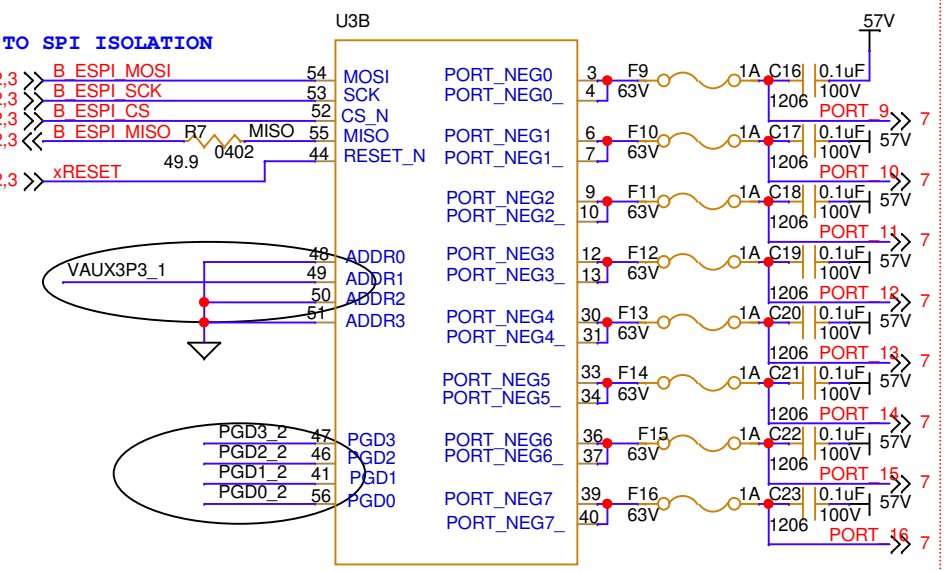
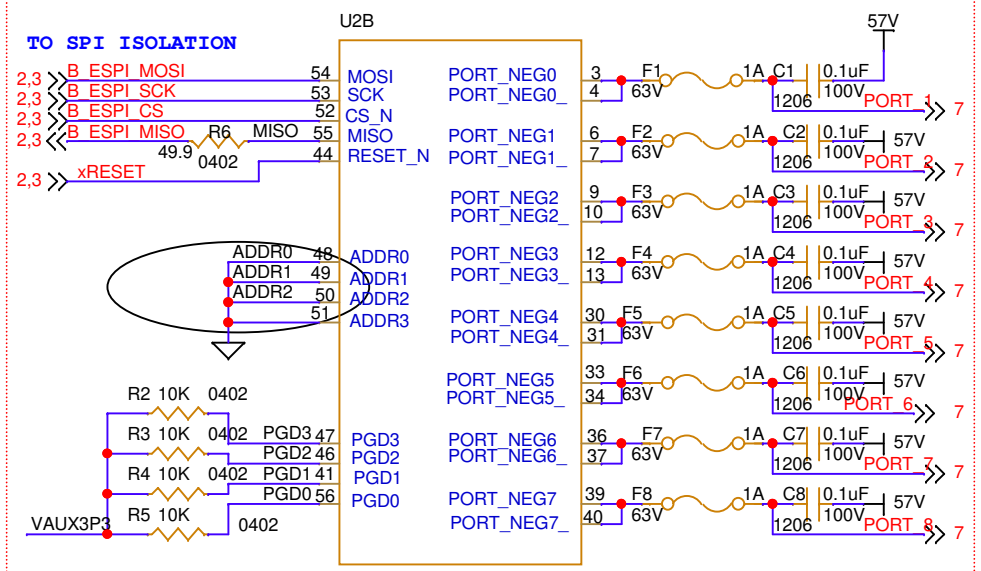


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mettre la résistance sur DGND?

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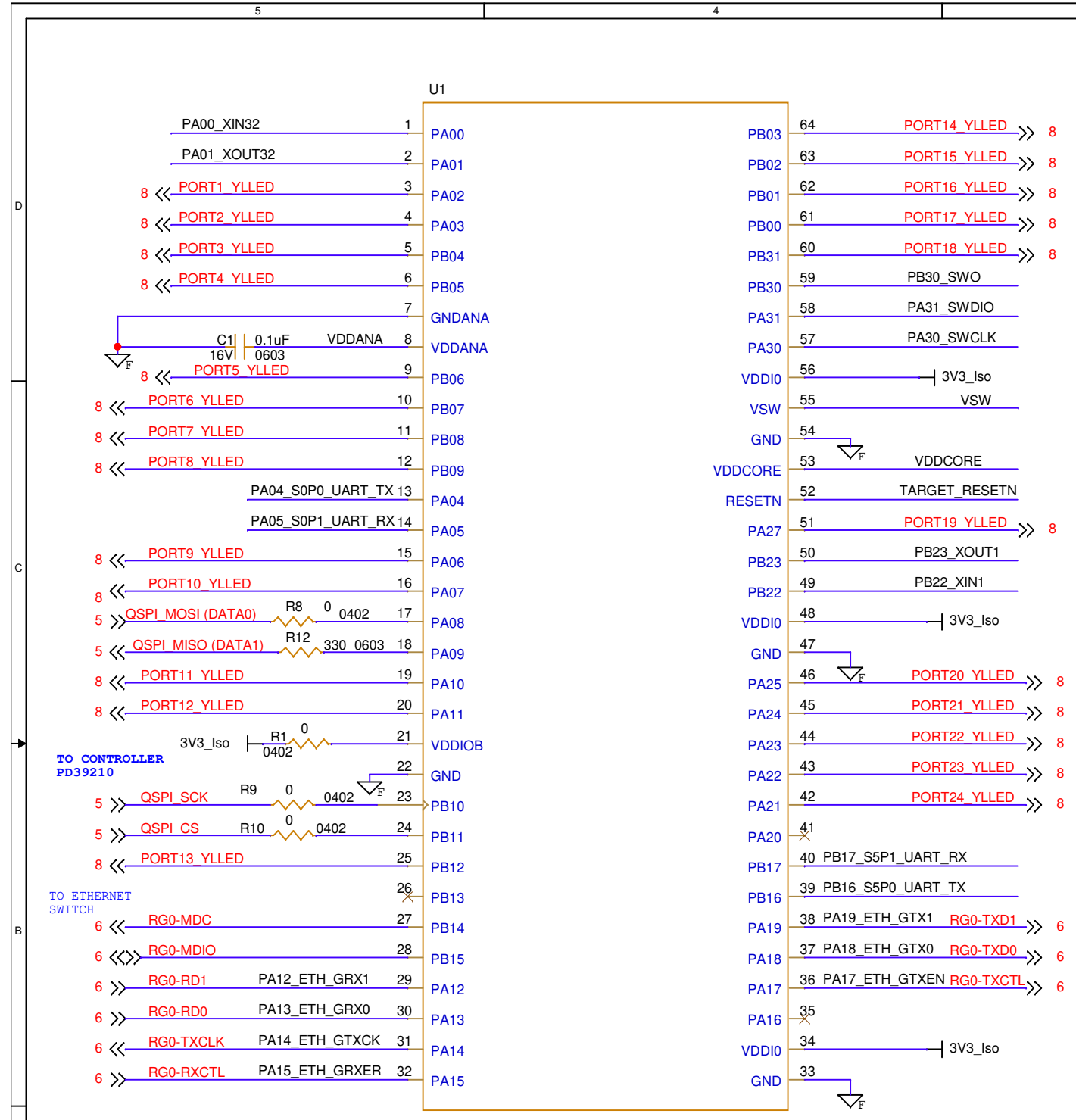
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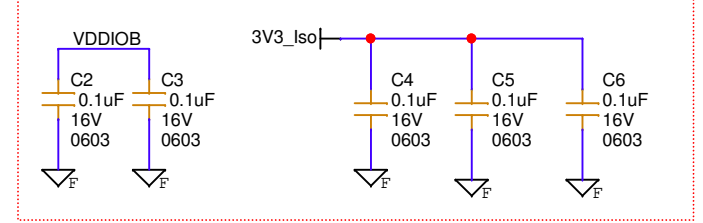
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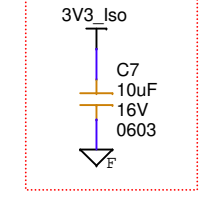


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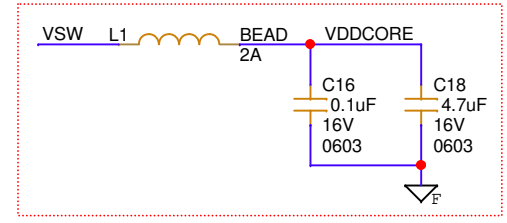
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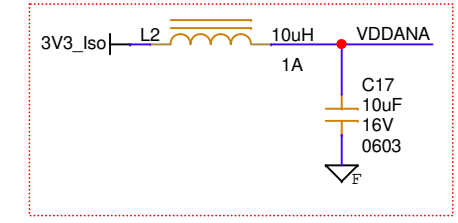
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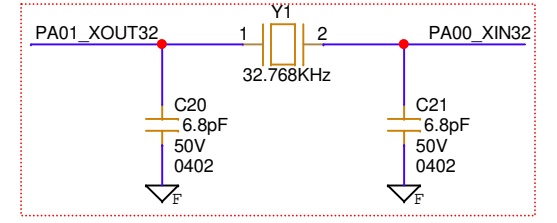
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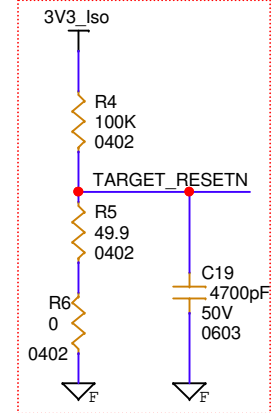
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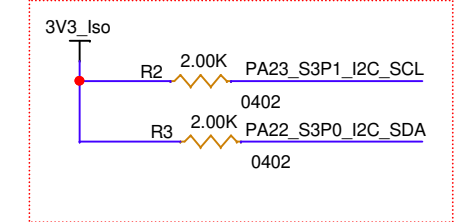
32.768 kHz Crystal



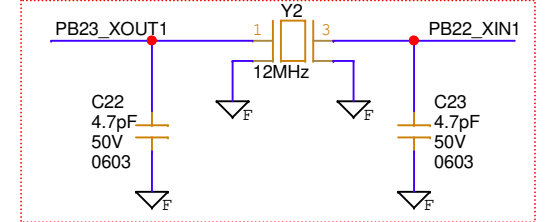
RESET with current limit and noise filter



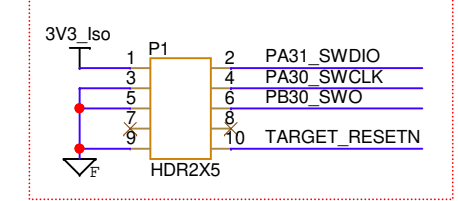
I2C PULL-UP



12 MHz Crystal



Connector for connecting an external programmer

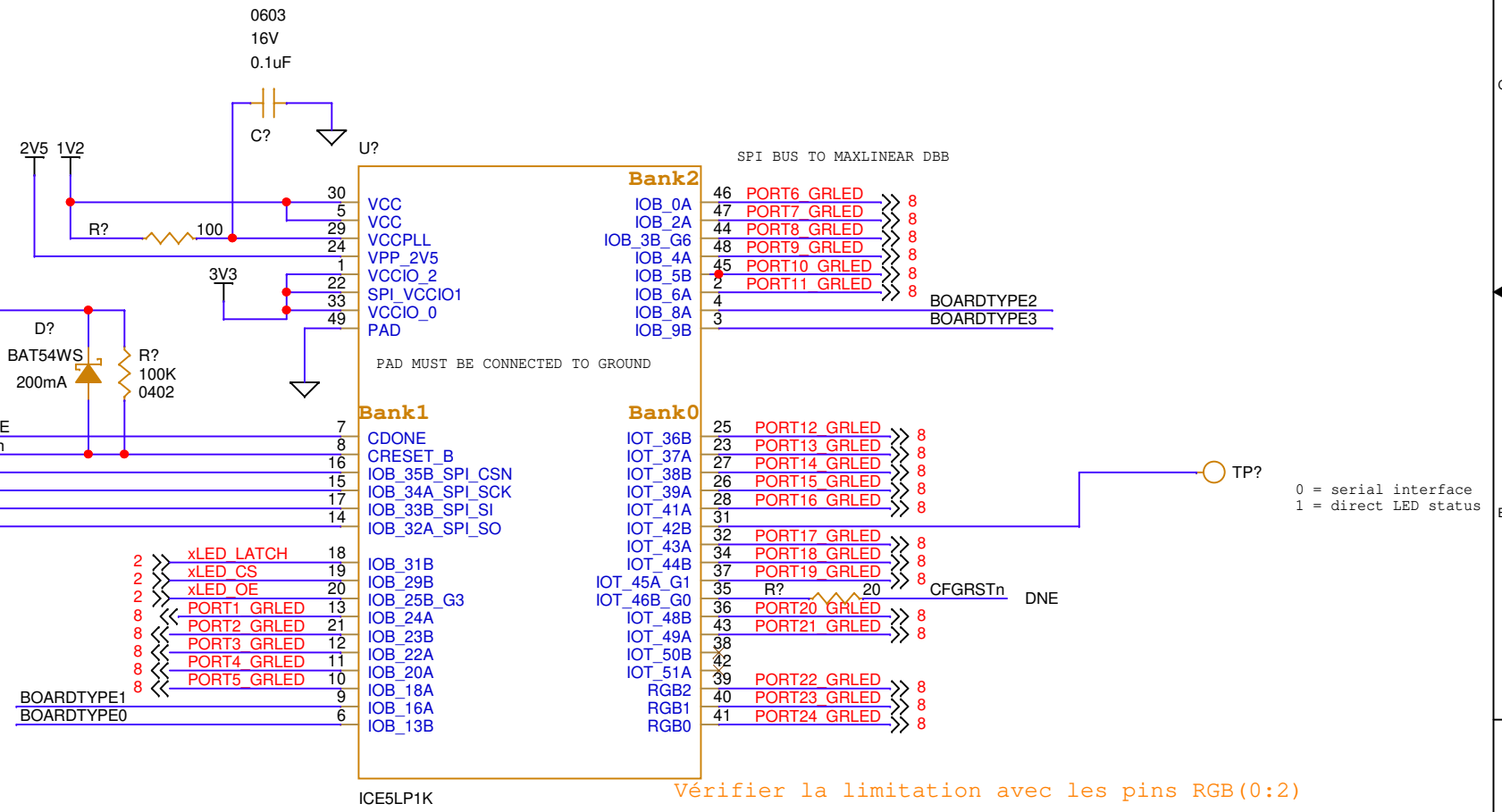
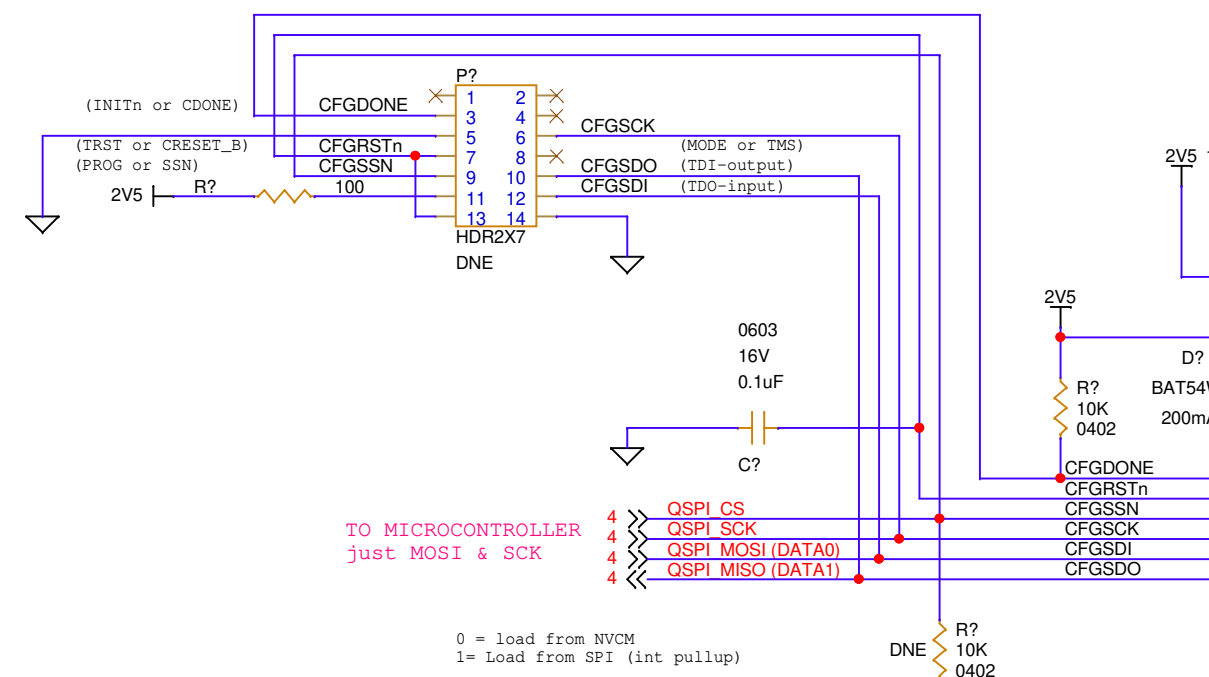
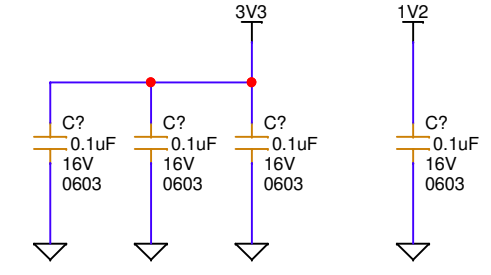
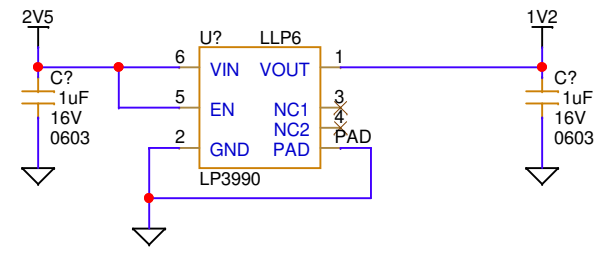
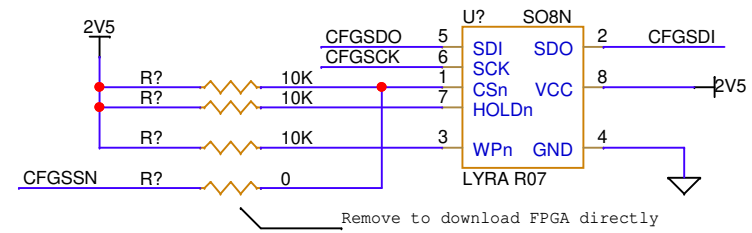


Il y a quelquechose de bizarre avec ce circuit

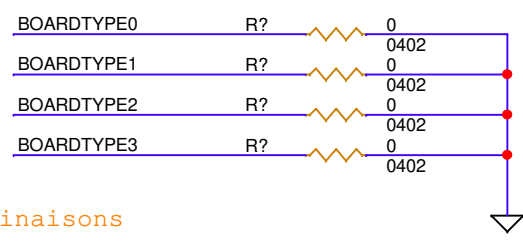
TO ETHERNET SWITCH

CARTOUCHE

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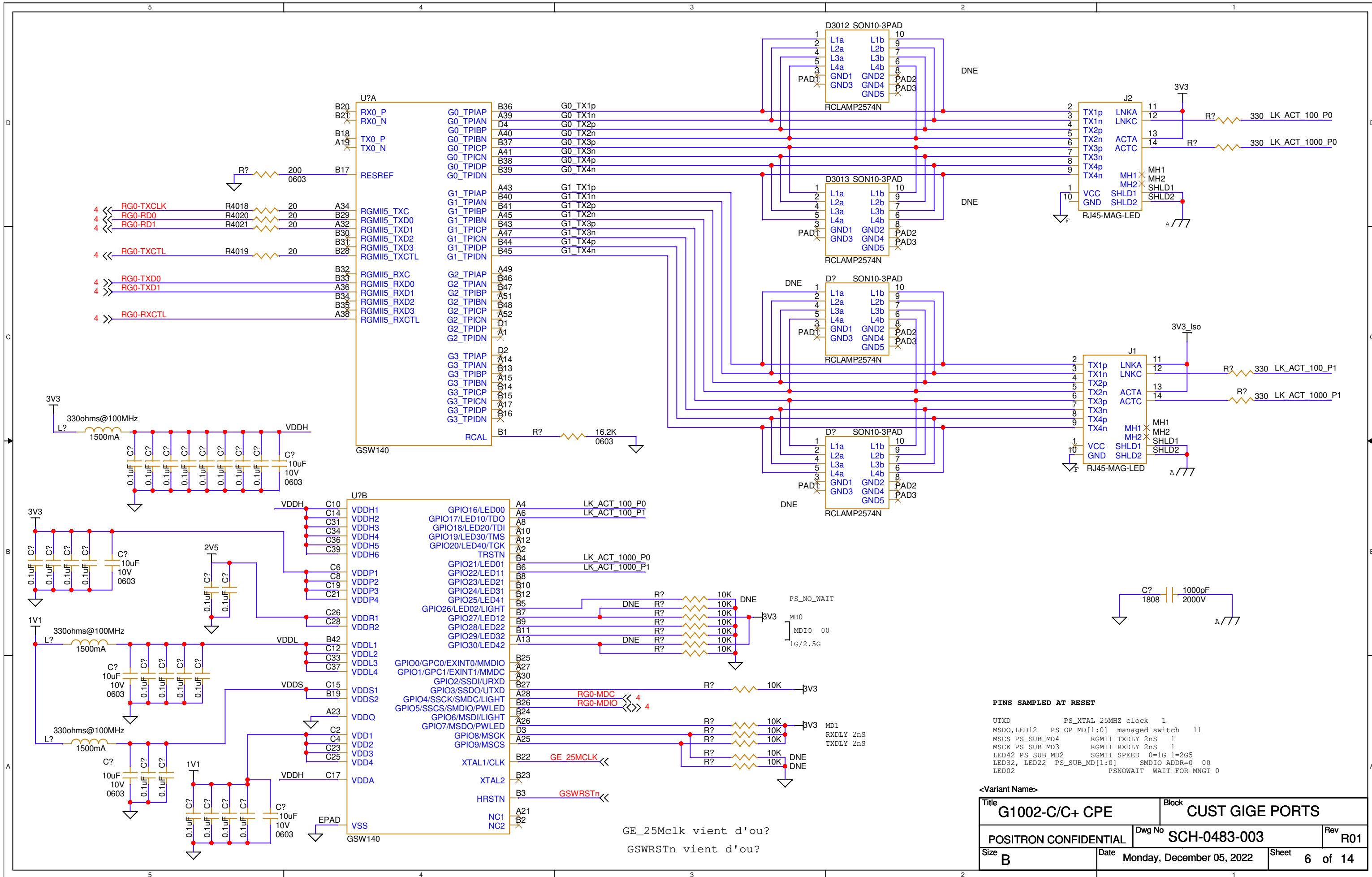
0 = load from NVCM  
1 = Load from SPI (int pullup)



Boardtype	Boardtype	Boardtype	Boardtype
0000	G1002-C	1000	TBD
0001	G1002-M	1001	TBD
0010	G1002-C+	1010	TBD
0011	G1002-M+	1011	TBD
0100	G1004-C	1100	TBD
0101	G1004-M	1101	TBD
0110	G1004-C+	1110	TBD
0111	G1004-M+	1111	G2002-M+

Il faut revoir si on a besoin d'autant de combinaisons

Title <b>G1002-C/C+ CPE</b>		Block <b>LYRA FPGA</b>	
POSITRON CONFIDENTIAL		Dwg No <b>SCH-0483-003</b>	Rev <b>R01</b>
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**PINS SAMPLED AT RESET**

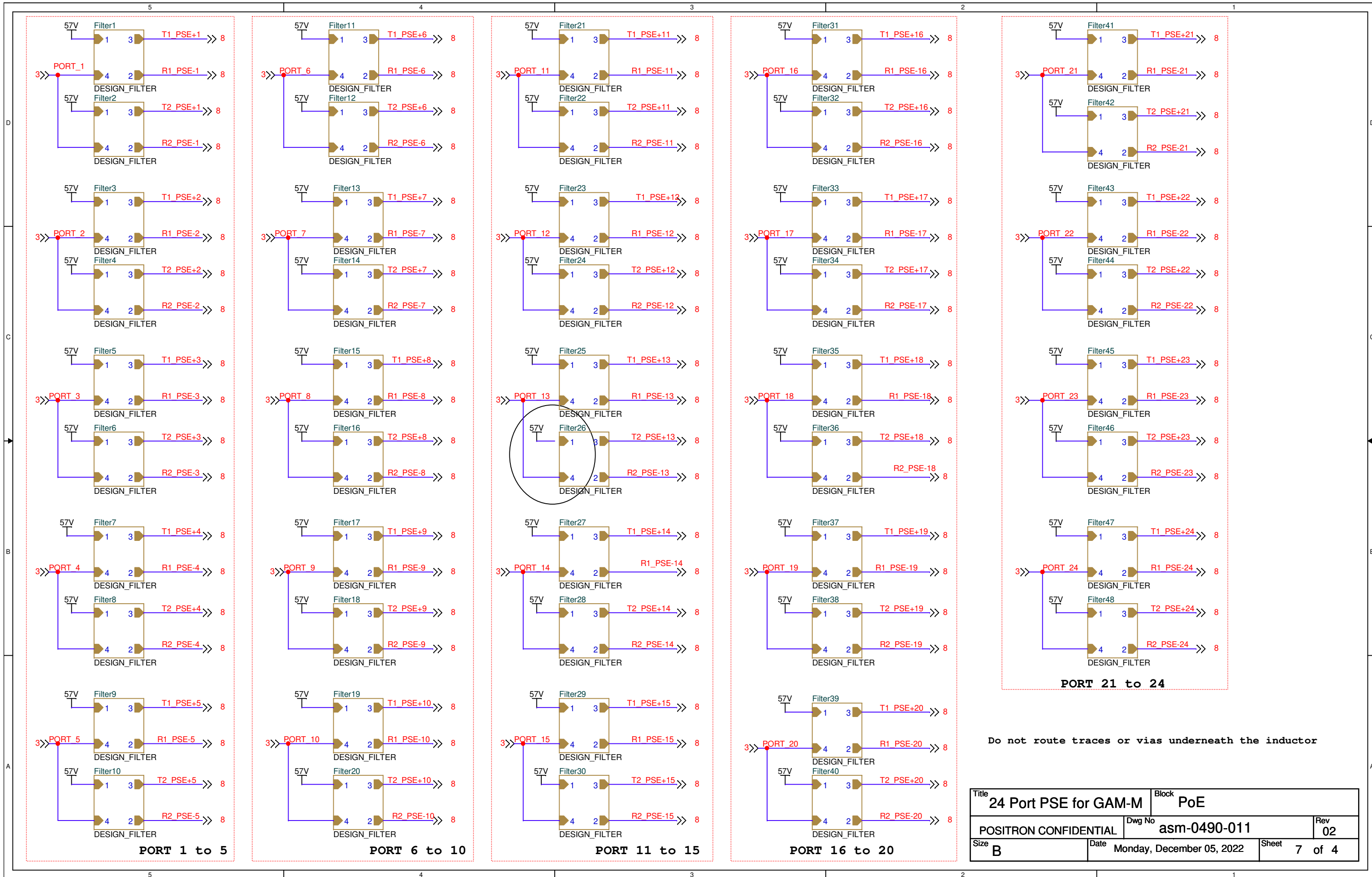
```

UTXD      PS_XTAL 25MHz clock 1
MSDO,LED12 PS_OP_MD[1:0] managed switch 11
MSCS PS_SUB_MD4 RGMII TXDLY 2ns 1
MSCK PS_SUB_MD3 RGMII RXDLY 2ns 1
LED42 PS_SUB_MD2 SGMII SPEED 0=1G 1=2G5
LED32, LED22 PS_SUB_MD[1:0] SMDIO ADDR=0 00
LED02      PSNOWAIT WAIT FOR MNGT 0
  
```

Title <b>G1002-C/C+ CPE</b>		Block <b>CUST GIGE PORTS</b>	
POSITRON CONFIDENTIAL		Dwg No <b>SCH-0483-003</b>	Rev <b>R01</b>
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GE\_25Mclk vient d'ou?  
GSWRSTn vient d'ou?

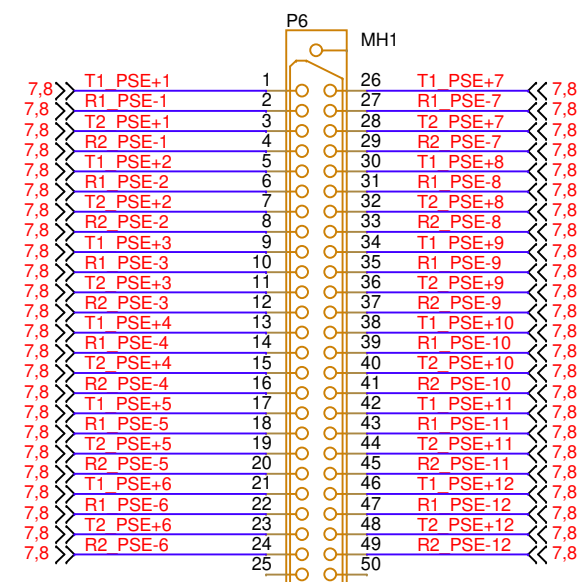
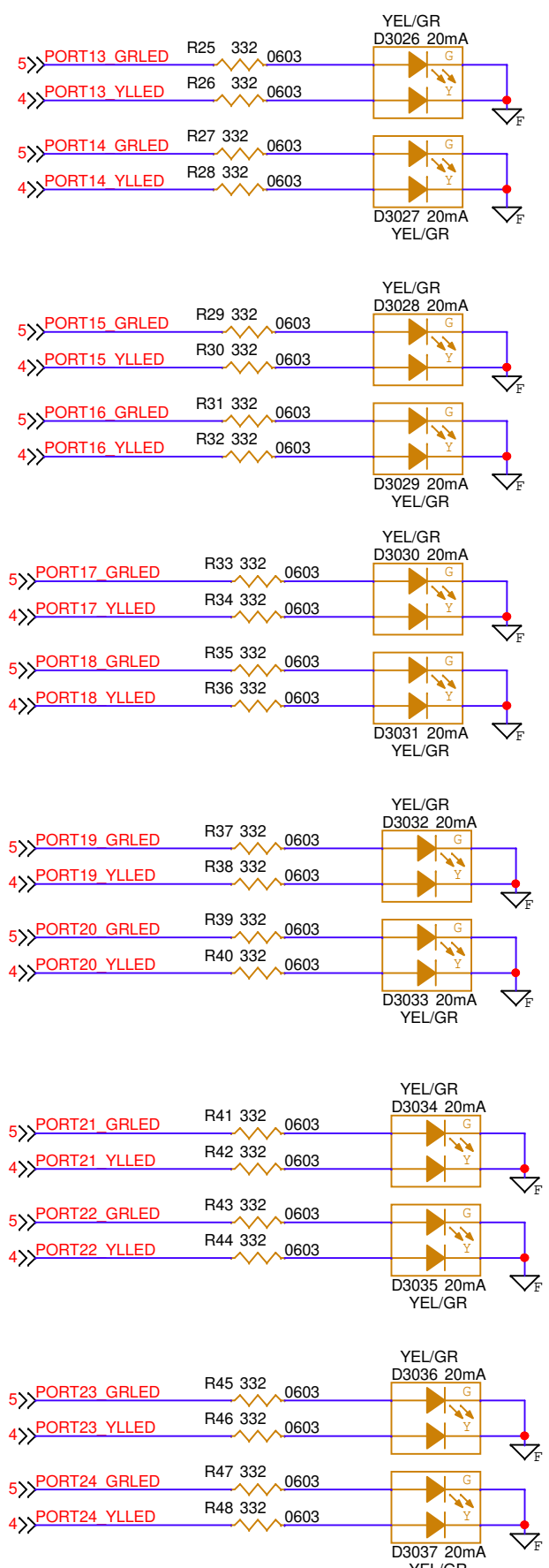
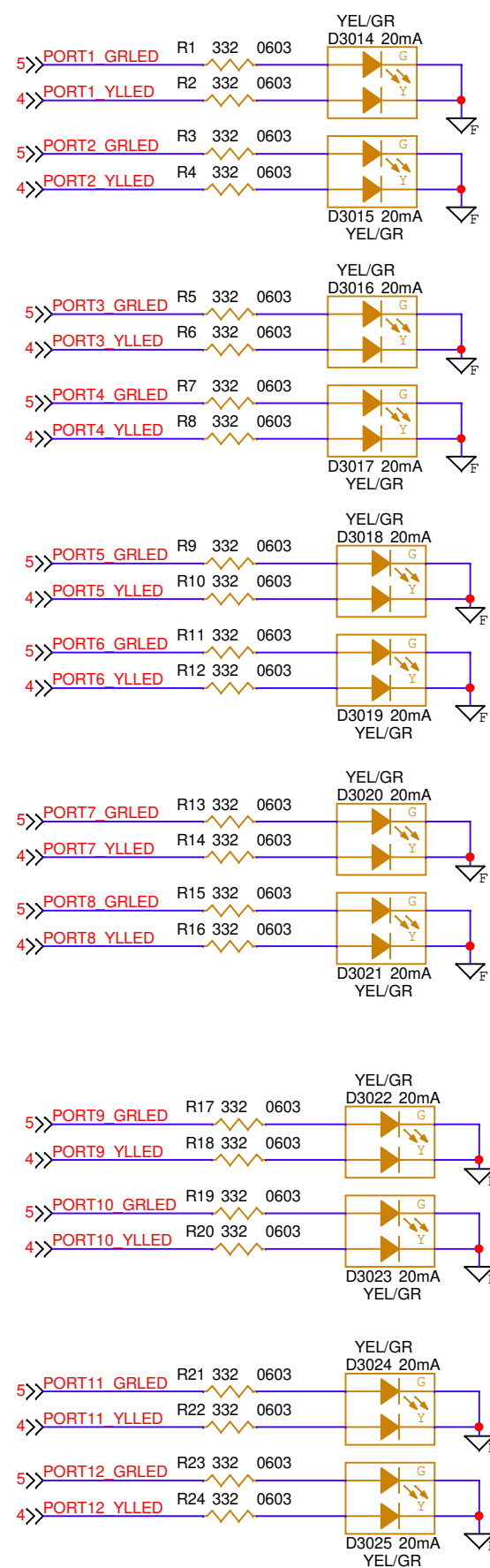




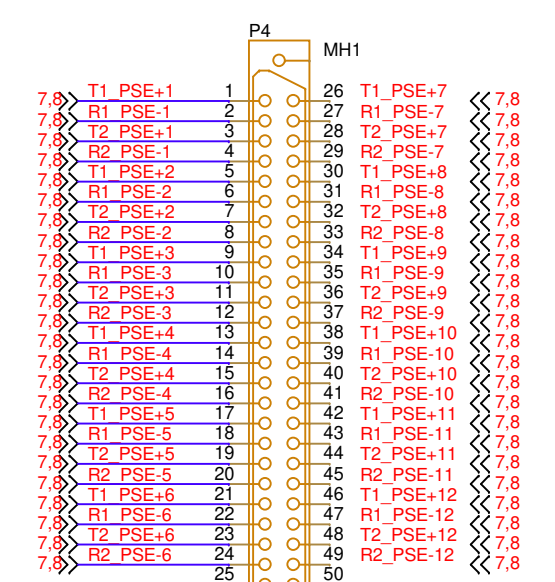
Do not route traces or vias underneath the inductor

Title <b>24 Port PSE for GAM-M</b>		Block <b>PoE</b>	
POSITRON CONFIDENTIAL		Dwg No <b>asm-0490-011</b>	Rev <b>02</b>
Size <b>B</b>	Date Monday, December 05, 2022	Sheet 7 of 4	

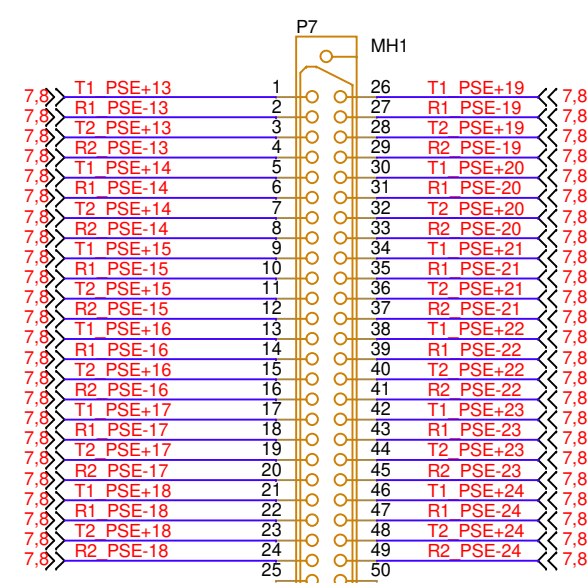




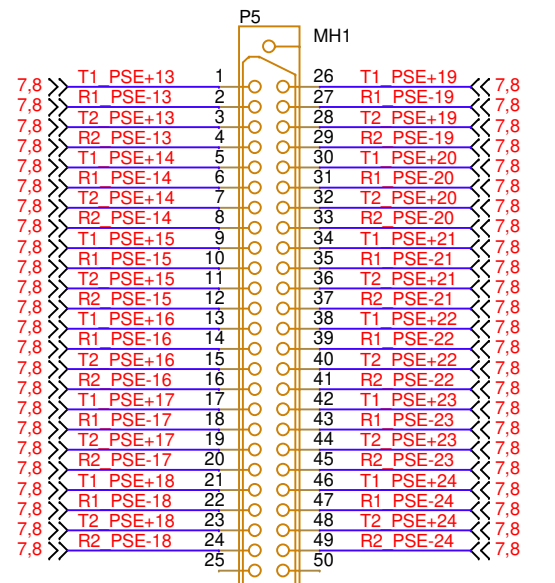
Mauvais pinout pour RJ21 (À corriger)  
 1=Rx\_1\_1, 26=Tx\_1\_1  
 2=Rx\_1\_2, 27=Tx\_1\_2...



Il manque les attributs DIFFERENTIAL\_PAIR



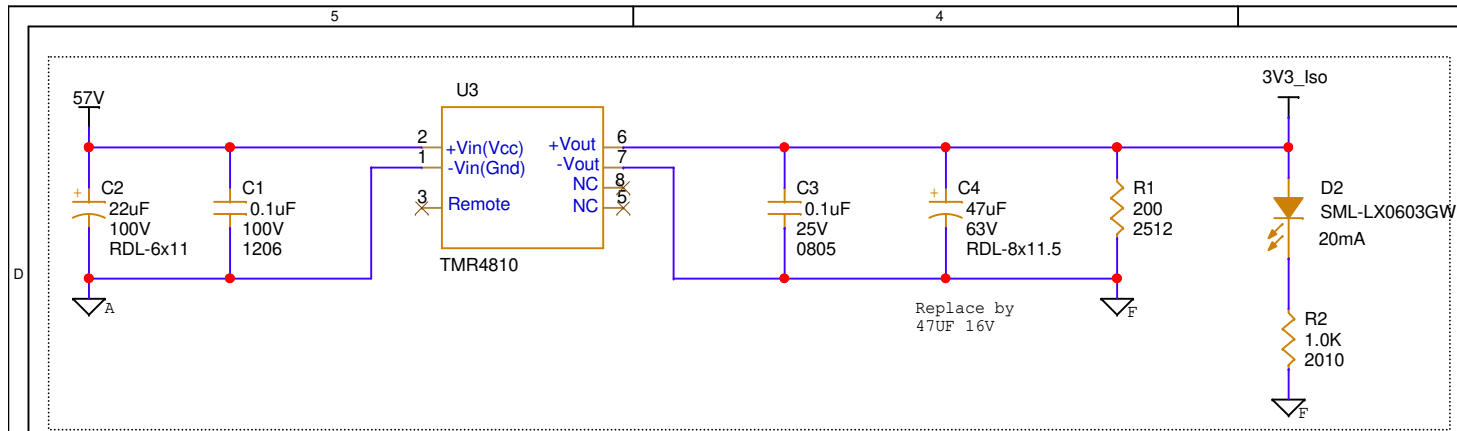
TELCO-M-ST-2X25-SD  
 Plug - Front Side



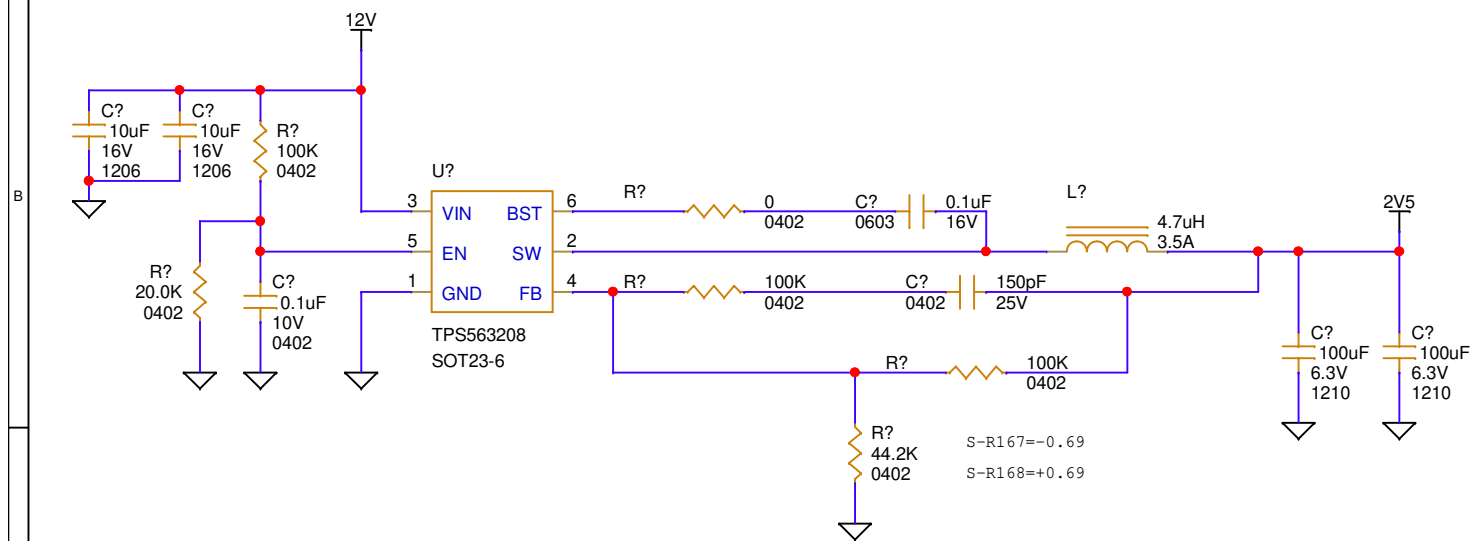
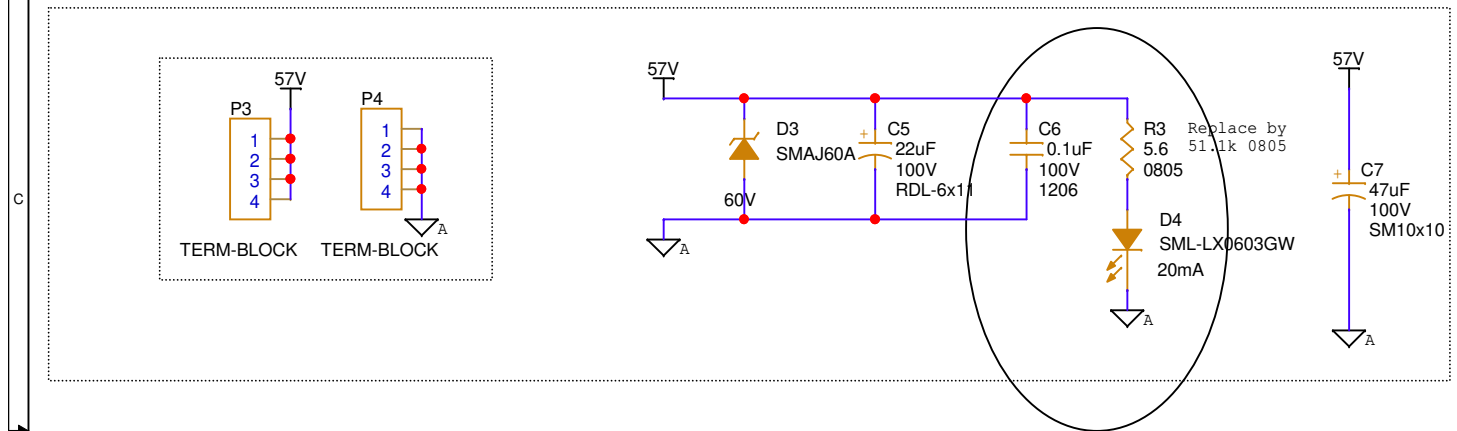
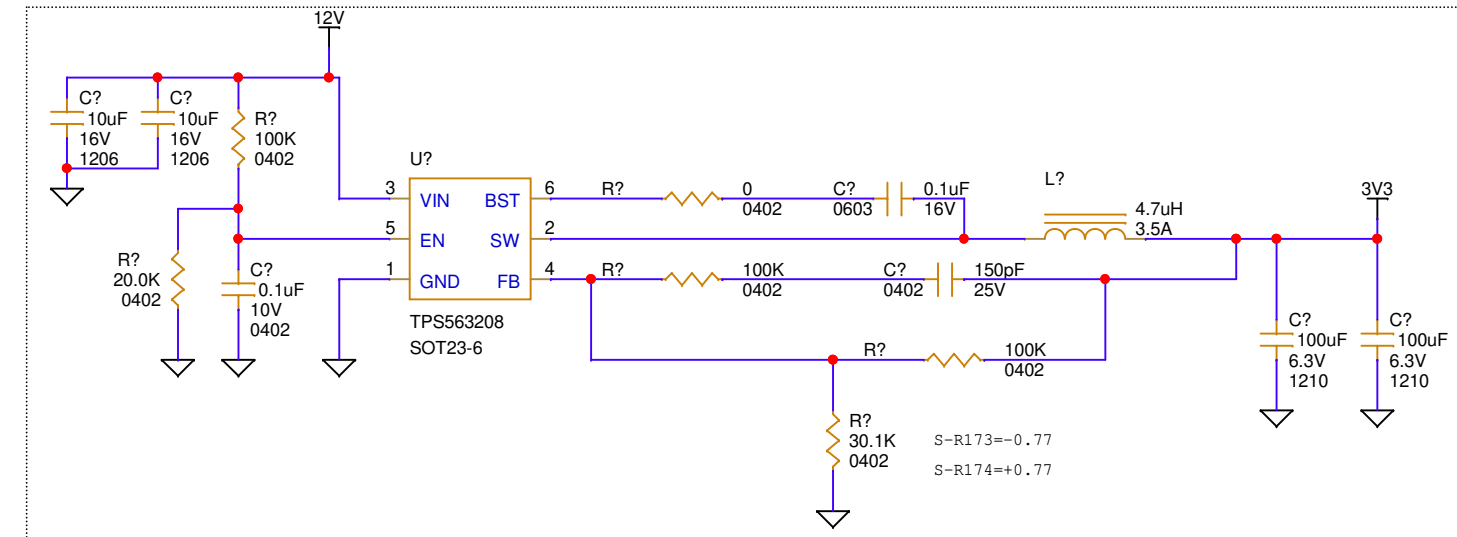
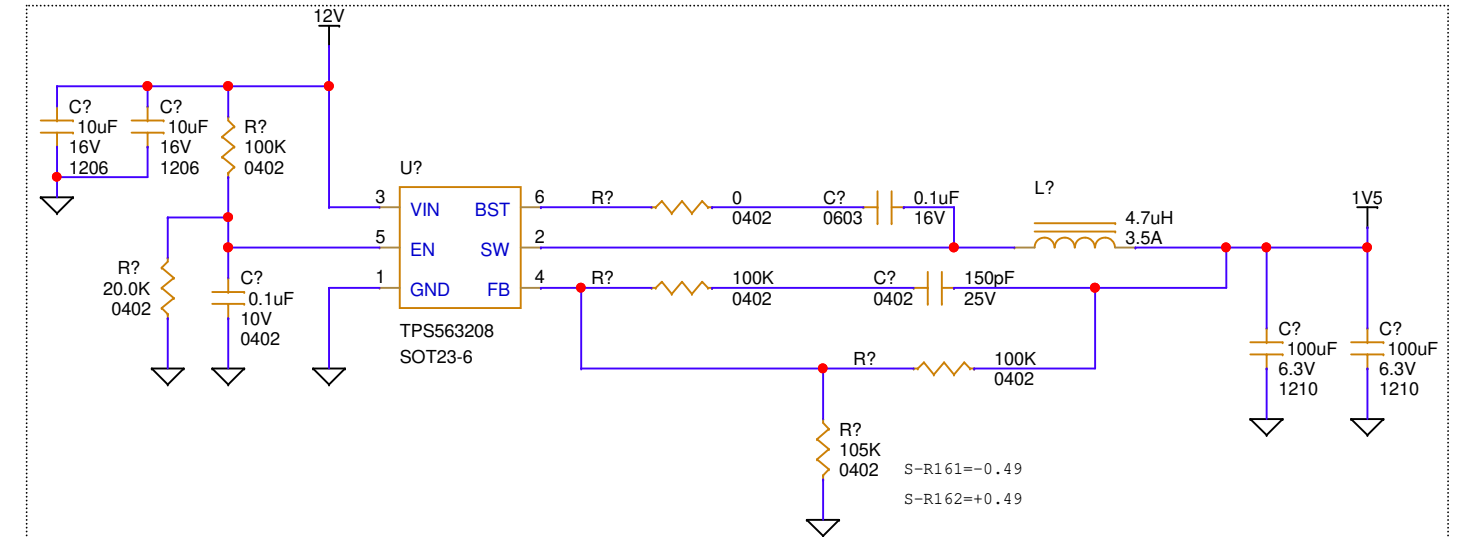
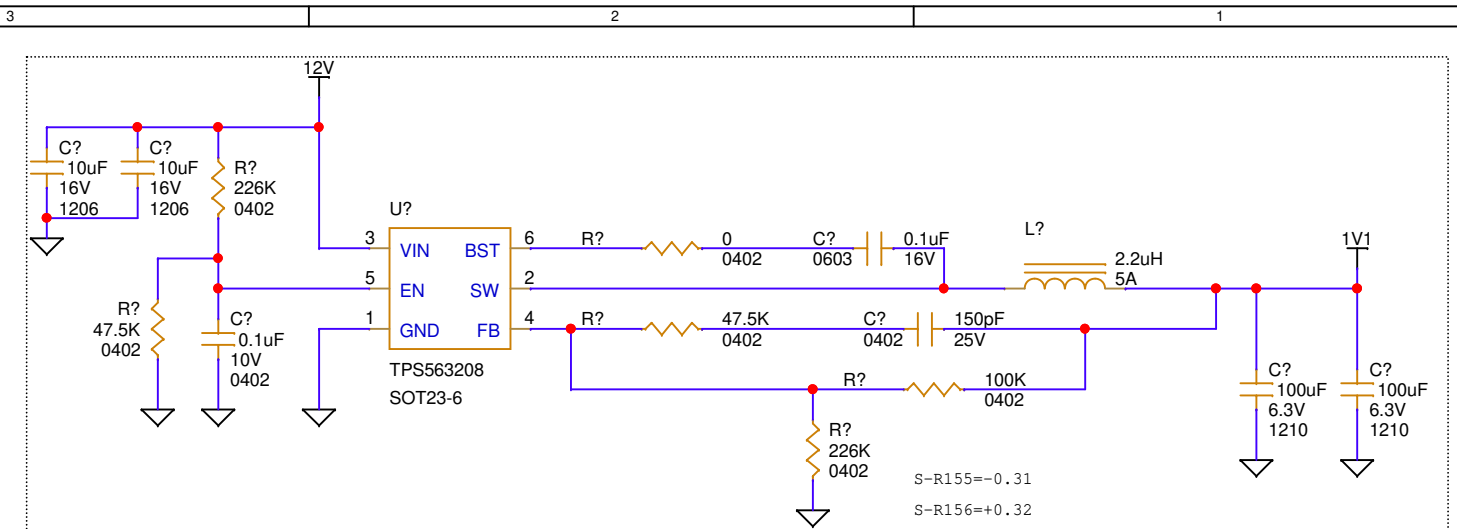
TELCO-F-ST-2X25-SD  
 Receptacle - Rear Side

Green LED from FPGA  
 Yellow LED from Microcontroller

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Trop couteux - Design avec composants discretes



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