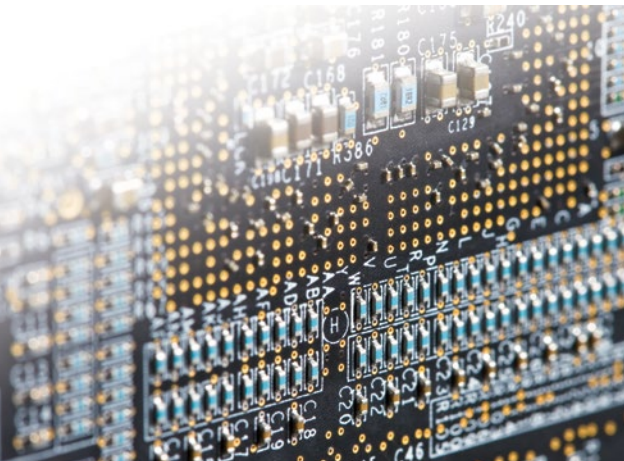




# Appendix A: 100+ PCB Design Guidelines to Minimize Signal Integrity Problems



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For more tips, tricks, design guidelines and signal integrity principles, visit: [www.signalintegrityacademy.com](http://www.signalintegrityacademy.com)



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## Warnings:

Never follow a rule blindly.

Always understand its origin and assumptions, and put in the numbers to evaluate its cost/benefit for your specific design. It's always a good habit to implement a design feature if it improves performance and is free.

If a design guideline will cost extra, you must estimate the impact to evaluate whether it is worth it.

## Warnings:

Always use rules of thumb or approximations to initially estimate a performance impact. If the result raises a flag or is close to a concern, this is motivation to pay extra to use a numerical simulation for a more accurate analysis.

Never use a rise time shorter than you need to, consistent with meeting timing budgets.

# Minimize Signal Quality Problems on One Net

**Strategy:** *Keep the instantaneous impedance the signal sees constant throughout its entire path.*

## **Tactics:**

0. Use controlled impedance traces.
1. Ideally, all signals should use the Vss or gnd planes as their return planes so there is an option of placing return vias to reduce plane resonances.
2. When a signal transitions from one return plane to another, if it is free, add a return via in as close proximity as practical.
3. To eliminate plane resonances, place shorting vias no farther than  $1/6$  a wavelength of the lowest frequency that might resonate. This is a spacing in inches  $\sim 1/(f \text{ in GHz})$

4. If different voltage planes are used as signal references, there should be tight coupling between the different voltage planes by keeping as thin a dielectric thickness between the layers as you can afford.
5. If different voltage return planes, add multiple, low inductance decoupling capacitors between the different voltage planes when a signal transitions. This will be the best of bad alternatives.
6. Use a 2D field solver to calculate the stack up design rules for the target characteristic impedance. Include the effects of solder mask and trace thickness.
7. Use series termination for point to point topologies, either single or bidirectional if it is consistent with timing analysis.
8. Terminate both ends of the bus in a multi-drop buss.

9. For data rates above about 2 Gbps, only point to point routing will work.
10. Keep the TD of stubs less than 20% the rise time of the fastest signals.
11. Place the series terminating resistors as close to the package pads as possible.
12. Use flyby termination for far end termination
13. Best termination of all is on-die termination.
14. Don't worry about corners unless 10 fF of capacitance is important.
15. Follow the return path of each signal and keep the width of the return path under each signal path at least as wide as the signal trace, and preferably at least 3 times as wide.
16. Route signal traces around return path discontinuities rather than across them.



17. Avoid using engineering change wires in any signal path.
18. Keep all non uniform regions as short as possible.
19. Do not use axial lead terminating resistors for system rise times less than 1 nsec. Use SMT resistors and mount them for minimum loop inductance.
20. When rise times are less than 150 psec, do everything possible to minimize the loop inductance of the terminating SMT resistors, or consider using integrated or embedded resistors
21. Vias generally look capacitive. Minimizing the capture pads and increasing the antipad clearance diameter will help make the via look transparent.
22. Consider adding a little capacitance to the pads of a low cost connector to compensate for its typically higher inductance.

23. Route all differential pairs with a constant differential impedance.
24. Avoid all asymmetries in a differential pair. Whatever you do to one trace, do the same to the other.
25. If the spacing between the traces in a differential pair has to change, adjust the line width to keep a constant differential impedance.
26. Add a compensation length to the short line in a differential pair in proximity to where the length asymmetry is created.
27. It is ok to change the coupling in a differential pair as long as the differential impedance is maintained.
28. In general, route differential pair traces with as tight a coupling as practical for highest interconnect density and lowest cost.

29. If data rates are above 5 Gbps or long lines, consider loosely coupled to enable wider lines and lower loss.
30. Broadside coupled differential pairs are rarely better than edge coupled. To use broadside coupled, you need a very compelling reason.
31. For any board level differential pairs, there will be significant return current in the planes, so avoid all discontinuities in the return path. If there is a discontinuity, do exactly the same thing to each line in the pair.
32. The only case to worry about terminating the common signals is if the common mode rejection ratio of the receiver is poor or if the reflecting common signals affect the eye quality. Terminating the common signals will not eliminate the common signal, just minimize its ringing.

33. If losses are important, use as wide a signal trace as possible and never less than 5 mils.
34. If losses are important, keep traces as short as possible.
35. If losses are important, do everything possible to minimize all capacitive discontinuities.
36. If losses are important, engineer the signal vias to look like 100 Ohms differential impedance, which usually means do everything possible to decrease the barrel size, decrease the capture pad size and increase the antipad clearance holes.
37. Never use non-functional pads on the via pad stack.
38. If losses are important, use as low a dissipation factor laminate as you can afford.
39. Consider using pre-emphasis and equalization if losses are important.

# Minimize Cross Talk

**Strategy:** *Minimize mutual capacitance and mutual inductance between adjacent signal-return path pairs.*

## **Tactics:**

40. For transmission lines, keep the spacing between adjacent signal paths at least twice the line width for microstrip or stripline.
41. Minimize any discontinuities in the return path the signals might cross over.
42. If you have to cross a gap in the return path, only use differential pairs. Never cross a gap with single ended signals routed close together.

43. Don't fool your self into thinking a capacitor is a low impedance interconnect structure. Its impedance will look like a 1-2 nH inductor above 10 MHz. It makes a poor "short" across a gap.
44. For surface traces, keep the coupled lengths as short as possible and use as much solder mask as practical to minimize far end cross talk.
45. If far end cross talk is a problem, add a laminate layer to the top of the surface traces to make them embedded microstrip.
46. For long coupled lengths when far end cross talk may be a problem, route the traces in stripline.
47. If you can't keep the coupling length less than the saturation length, changing the coupling length will have no impact on the near end cross talk, so don't worry about decreasing coupling length.

48. Use the lowest dielectric constant laminate you can afford so the dielectric spacing to the return planes can be kept to a minimum for the same target characteristic impedance.
49. In a tightly coupled microstrip bus, the deterministic jitter can be reduced by keeping the spacing at least as wide as twice the line width or routing timing sensitive lines in stripline.
50. For isolations in excess of -60 dB, use stripline with guard traces.
51. Guard traces can often make cross talk larger in surface traces unless the traces are very short.
52. Always use a 2D field solver to evaluate whether you need to use a guard trace.

53. If you do use a guard trace in stripline, make it as wide as will fit and use vias to short it to the return path and spaced at least 3 vias per rise time.
54. Minimize ground bounce by making the return paths in any packages or connectors as short and as wide as possible.
55. Use chip scale packages rather than larger packages.
56. Minimize ground bounce in the power return path by bringing the power plane as close to the return plane as possible.
57. Minimize ground bounce in the signal return paths by bringing the signal path as close to the return path as acceptable, consistent with matching the impedance of the system.
58. Avoid using shared return paths in connectors and packages.



59. When assigning leads in a package or connector, reserve the shortest leads for the ground paths and space the power and ground leads uniformly among the signal paths, or closest to those signal paths that will carry a lot of switching current.
60. All no-connect leads or pins should be assigned as ground return connections.
61. Avoid using resistor SIPs unless there are separate return paths for each resistor.
62. Check the Gerbers to verify anti-pads in via fields do not overlap and there is a well defined web between clearance holes in the power and ground planes.

63. If a signal changes reference planes, the reference planes should be as closely spaced as you can afford. If you use a decoupling capacitor to minimize the impedance of the return path, its capacitance value is immaterial. Select it and design it in for lowest loop inductance.
64. If many signal lines switch reference planes, space the signal path vias as far apart as possible, rather than clustering them all in the same location.
65. If a signal switches reference layers, and they are the same voltage level, place a via between the return planes as close to the signal via as possible.

# Minimize Rail Collapse

**Strategy:** *Minimize the impedance of the power distribution network.*

## **Tactics:**

66. Minimize the loop inductance between the power and ground paths
67. Allocate power and ground planes on adjacent layers with as thin a dielectric as you can afford.
68. Get the lowest impedance between the planes by using as high a dielectric constant between the planes as you can afford consistent with the thinnest dielectric possible.
69. Use as many power and ground plane pairs in parallel as you can afford.

70. Route the same currents far apart and opposite currents close together
71. Place each power via as close as practical to a ground via. If you can't get them at least within a pitch equal to their length, there will be no coupling and no value in proximity.
72. Route the power and ground planes as close as possible to the surface where the decoupling capacitors are mounted.
73. Use multiple vias to the same power or ground pad but keep the vias as far apart as possible.
74. Use vias as large in diameter as practical when routing to power or ground planes.
75. Use double bonding on power and ground pads to minimize the loop inductance of the wire bonds.

76. Use as many power and ground connections from the chip as you can afford.
77. Use as many power and ground connections from the package as you can afford.
78. Use chip attach methods that are as short as possible, such as flip chip rather than wire bond.
79. Use package leads as short as possible, such as chip scale packages rather than QFP packages.
80. Keep all surface traces between the pads of the decoupling capacitors and their vias as short and wide as possible.
81. Use a total amount of bulk decoupling capacitance to take over from the regulator at low frequency.
82. Use a total number of decoupling capacitors to reduce the equivalent inductance at high frequency.

83. Use as small a body size decoupling capacitors as you can afford and minimize the length of all connections from the capacitor pads to the power and ground planes.
84. Place as much decoupling capacitance as you can afford on the chip itself.
85. Place as many low inductance decoupling capacitors as you can afford on the package.
86. Use differential pairs for I/Os.
87. The ONLY way of estimating the values and number of capacitors is using a simulation that includes the on-die capacitance and package lead inductance.
88. If you don't have any information about the package or chip, select capacitors and numbers to provide a flat impedance profile from 1 MHz to about 50 MHz.

# Minimize EMI

**Strategy:** *Reduce the voltage that drives common currents, increase the impedance of the common current paths, shield and filter as a band aide.*

## **Tactics:**

89. Reduce ground bounce by providing a low impedance, continuous return path under all signals, especially surface traces.
90. Keep all traces at least 5 line widths from the edge of the board
91. Route traces in stripline when possible.

92. Place the highest speed/highest current components as far from the I/O connections as possible.
93. Place the decoupling capacitors in proximity to the chips to minimize the spread of high frequency current components in the planes. Don't fool yourself into thinking capacitors provide low impedance above about 100 MHz.
94. Keep power and ground planes on adjacent layers as close together as possible.
95. Use as many power and ground plane pairs as you can afford.
96. When using multiple power and ground plane pairs, recess the power planes and stitch shorting vias between the ground planes along the edges.
97. Use ground planes as surface layers, where possible.



98. Know the resonant frequency of all packages and change the package geometry if there is an overlap with a clock harmonic.
99. Avoid signals switching different voltage reference planes in a package. This will drive package resonances.
100. Add ferrite filter sheets to the top of packages if they might have a resonance.
101. Minimize any asymmetries between the lines in each differential pair.
102. Use a common signal choke filter on all differential pair connections that leave the board.
103. Use a common signal choke filter around the outside of all peripheral cables.
104. Filter all external I/O lines to use the longest signal rise time that is tolerable for the timing budget.

105. Use spread spectrum clock generator to spread the first harmonic over a wider frequency range and decrease the radiated energy within the bandwidth of the FCC test.
106. When connecting shielded cables, try to keep the shield as an extension of the enclosure.
107. Minimize the inductance of the shielded cable connections to the enclosure. Use a coaxial connection right to the end of the cable and connecting to the enclosure.
108. Never use a pigtail connection between the cable shield and the chassis.
109. Equipment bays should not penetrate the integrity of the enclosure.
110. Only interconnects need to break the enclosure integrity.

111. Keep apertures small diameter, significantly smaller than a wavelength of the lowest frequency radiation that might leak. More smaller holes are better than fewer large holes.
112. The most expensive rule is the one that delays the product ship date.



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