10G PON Chipset

10G PON Development Kit
EASY PRX126 REF BOARD

PRX126 SFP+ Reference Board

V2.2.3 HW6.1.03

Hardware Design Guide

MaxLinear Confidential

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Preface

This document describes the 10G PON Development Kit EASY PRX126 REF BOARD V2.2.3, which is an SFP+ demonstration platform for the 10G PON Chipset PRX126 device.

The board is designed to be plugged into the Base Board EASY 98900 V2.2, or into any system with an SFP+ connector.

This document uses these synonyms to simplify matters:

EASY PRX126 REF BOARD

Synonym used for the 10G PON Development Kit EASY PRX126 REF BOARD V2.2.3

PRX126

Synonym used for the 10G PON Chipset PRX126

EASY 98900

Synonym used for the Base Board EASY 98900 V2.2

Organization of this Document

- **Chapter 1**, **Overview**
  This chapter provides an overview of the features of the EASY PRX126 REF BOARD.
- **Chapter 2**, **Interfaces and Pinout**
  This chapter describes the interfaces of the EASY PRX126 REF BOARD.
- **Chapter 3**, **Mode Settings**
  This chapter describes the special modes used to debug and test the EASY PRX126 REF BOARD.
- **Chapter 4**, **EASY PRX126 REF BOARD Dimension Drawing**
  This chapter provides the dimension drawing and floorplan of the EASY PRX126 REF BOARD.
- **Literature References** and **Standards References**
- **Terminology**

1 Overview

The PRX126 is a member of the 10G PON Chipset family of 10G PON Optical Network Unit (ONU) devices. The EASY PRX126 REF BOARD provides an example of the compact density achievable with a PRX126 design. **Figure 1** shows the EASY PRX126 REF BOARD with and without its case.

Figure 1 EASY PRX126 REF BOARD with and without External Case

Figure 2 shows the EASY PRX126 REF BOARD and the Base Board EASY 98900. The EASY 98900 includes a Marvell* AQR107 10 Gbps Ethernet PHY and an Atmel* ATMega328 microcontroller.

The EASY PRX126 REF BOARD only requires one external power supply of 3.3 V (see **Section 1.5**). The 3.3 V supply for the PRX126 is provided by the SFP Base Board via the SFP edge connector. The SFP Base Board requires an external 12 V supply.

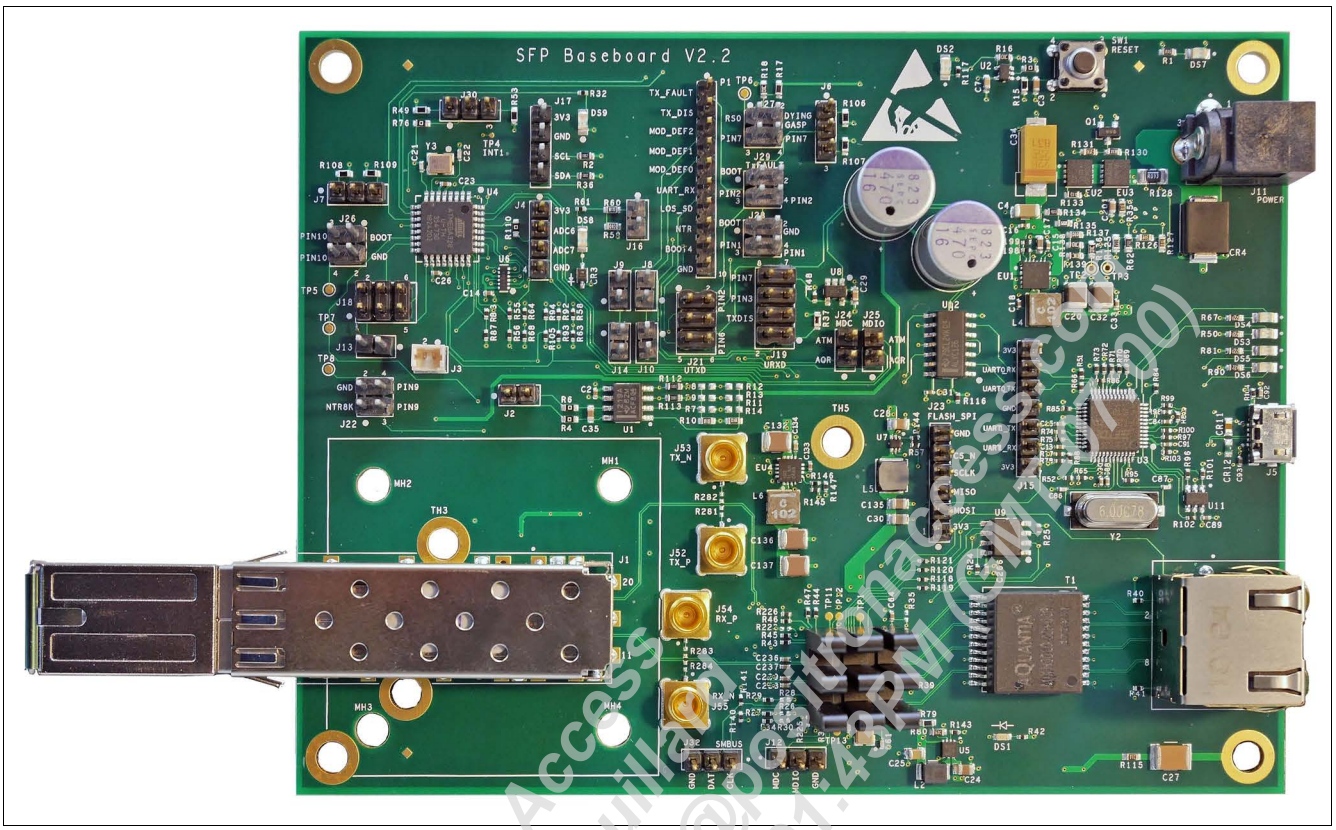

Figure 2 EASY PRX126 REF BOARD Inserted into the EASY 98900 Base Board

1.1 Block Diagram

Figure 2 shows the EASY PRX126 REF BOARD block diagram which consists of these components:

- PRX126 soldered onto the EASY PRX126 REF BOARD
- SFP connector (edge connector)
- Optical receptacle (BOSA)
- LPDDR3 SDRAM
- DC/DC converter and LDO
- Avalanche photodiode (APD)
- Current mirror circuitry

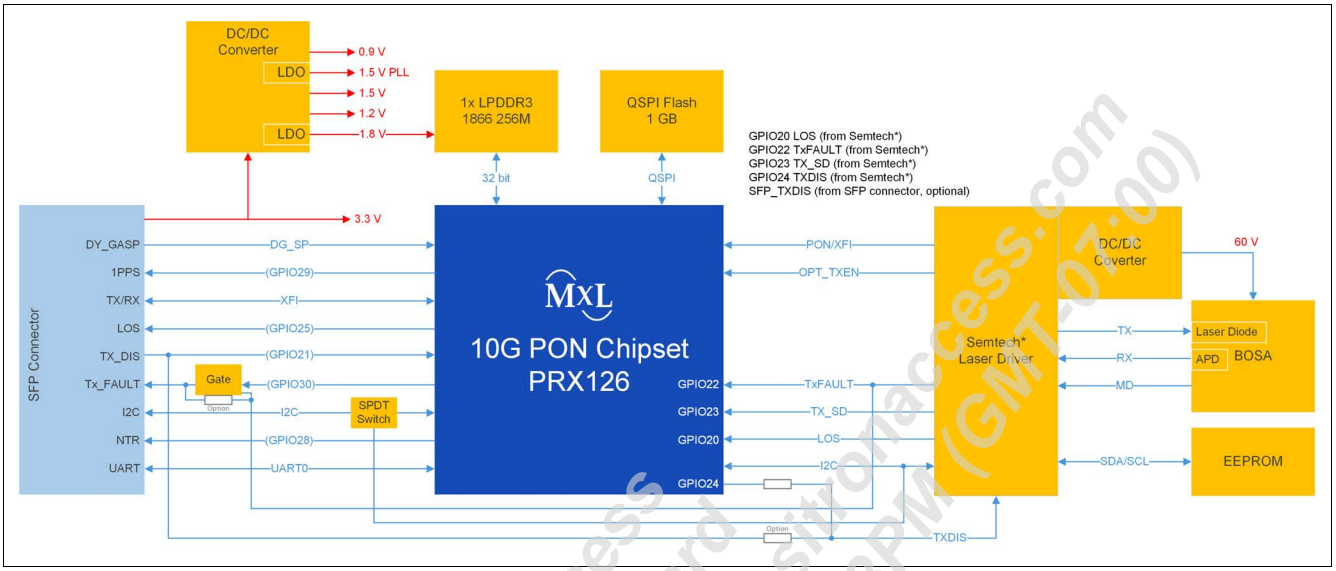

Figure 3 EASY PRX126 REF BOARD Block Diagram

1.2 PRX126

The main component of the EASY PRX126 REF BOARD is the PRX126. The pinout and package of this device are optimized for an SFP+ design.

1.3 BOSA

The external circuitry and layout are optimized for the specific BOSA used in the design, which is from an EZconn Corporation* EBS666272-B3. Since the BOSA does not provide an RSSI output, there is a current mirror circuit on the EASY PRX126 REF BOARD (see **Section 1.4**).

1.4 APD and Current Mirror Circuitry

A laser driver is not included in the PRX126. A Semtech* GN28L96-QFN-TR Physical Media Dependent (PMD) device is included on the EASY PRX126 REF BOARD. This PMD generates the APD voltage for the BOSA.

The PMD device controls a DC/DC converter for the APD, which generates the voltage for the BOSA. The voltage is between 30 V and 48 V. The current mirror circuit is connected to the output of the DC/DC converter for the APD and provides an RSSI signal to the PMD device.

1.5 Power Supply

The edge connector provides the EASY PRX126 REF BOARD with a 3.3 V power supply via two pins. The DC/DC converter on the EASY PRX126 REF BOARD uses this supply to generate the 0.85 V core voltage for the PRX126.

The LPDDR3 SDRAM power supply of 1.2 V is provided by a DC/DC converter and 1.5 V is provided by an LDO. All voltages are generated from the 3.3 V supplied via an SFP connector.

1.6 Memory

The EASY PRX126 REF BOARD has a NAND flash memory device and an LPDDR3 SDRAM device on board. The NAND flash memory is used to boot the software and to save some register values. An 8 Gbit LPDDR3 device is used in the design, but a 4 Gbit device is also allowed. The transfer rate of the LPDDR3 is 1866 Mtps. A 1 GByte QSPI flash memory device is used to store the operating system and is supplied by the 1.8 V power supply.

2 Interfaces and Pinout

This chapter describes the SFP connector and optical interfaces on the EASY PRX126 REF BOARD.

2.1 SFP Connector (J1)

The SFP connector (J1) layout and pin-pad placement comply with the Multi-Source Agreement (MSA) Group specification [4].

Some pins have varying functions depending on modes selected via software (refer to [2]). During software development, it is possibly necessary to access the internal registers of the PRX126 for debugging. For this purpose, the two signal pins TxFault and Rate_Select are connected to GPIOs on the PRX126. These GPIOs are usable as an asynchronous serial interface (ASC).

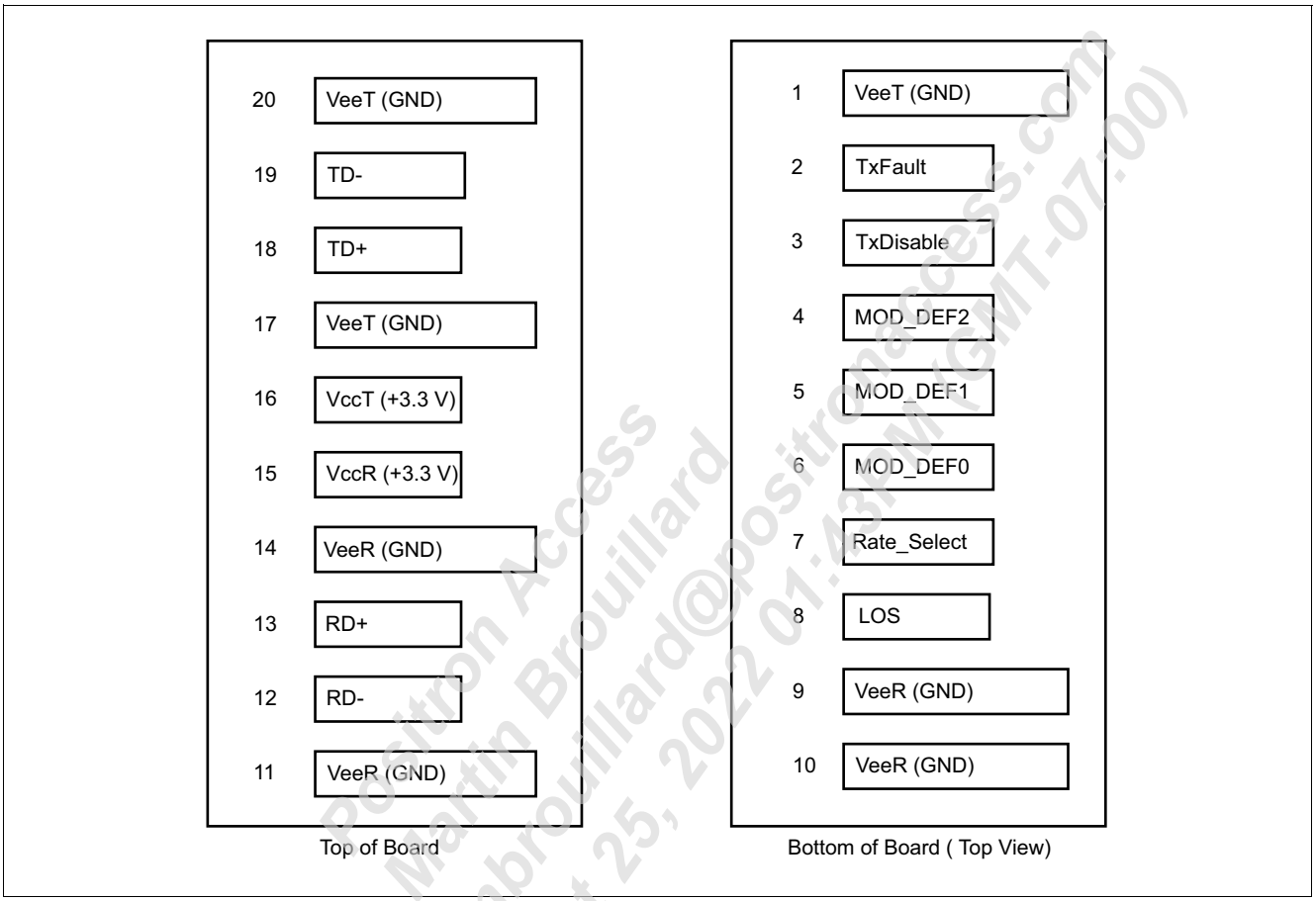

Figure 4 SFP Connector J1

Table 1 SFP Connector J1

Pin	Use	SFP Function	SFP+ Function	Connected to PRX126 Signal Pin
1	I/O	VeeT	VeeT	GND
2	O	TxFault	TxFault	UART_TX, GPIO28 (NTR), GPIO31 (BOOT), TxFAULT from MACOM* PMD via U2 or GPIO30 (TxFAULT, option)
3	I	TxDisable	TxDisable	GPIO21
4	I/O	MOD_DEF2	I2C_SDA	GPIO11
5	I	MOD_DEF1	I2C_SCL	GPIO10

Table 1 SFP Connector J1 (cont'd)

Pin	Use	SFP Function	SFP+ Function	Connected to PRX126 Signal Pin
6	I/O	MOD_DEF0	MOD_ABS	GPIO8
7	I	Rate Select	RS0	UART0_RX, DY_GSP
8	O	LOS	LOS	GPIO25
9	I/O	VeeR	RS1	GND or GPIO29
10	I	VeeR	VeeR	GND or GPIO16
11	I	VeeR	VeeR	GND
12	O	RD-	RD-	SI_TXD_N
13	O	RD+	RD+	SI_TXD_P
14	O	VeeR	VeeR	GND
15	O	VccR	VccR	+3.3 V
16	I/O	VccT	VccT	+3.3 V
17	I/O	VeeT	VeeT	GND
18	I	TD+	TD+	SI_RXD_P
19	I	TD-	TD-	SI_RXD_N
20	I/O	VeeT	VeeT	GND

The special or second functions for the signals are specified in the Table 2. These special functions are set via software. This excludes the boot pins BOOT3, BOOT2, and BOOT1, which have to be set via jumpers on the SFP Base Board.

Table 2 Special Functions of SFP Connector Pins on J1

Pin	Use	Standard Function	Special Function 1	Description	Special Function 2	Description
2	I/O	TxFault	TxFAULT, BOOT and UART_TX	Boot mode and debug	NTR	Network Timing Reference
4	I/O	MOD_DEF2	I2C_SDA	-	-	-
5	I	MOD_DEF1	I2C_SCL	-	-	-
7	I	Rate Select	DY_GASP or UART0_RX	Dying gasp or debug	-	-
8	O	LOS	-	-	-	Pulses per second
9	O	GND	PPS	Pulses per second	-	-
10	I	VeeR	BOOT0	Boot mode	-	-

Table 3 specifies the special function modes of boot pins 2 and 10.

Table 3 Boot Mode Setup on J1

BOOT3 and BOOT2	BOOT1	Boot Mode
+3.3 V	GND	Standard boot via internal quad SPI flash memory
GND	GND	Boot via ASC interface

2.2 Optical Receptacle

The BOSA included in the EASY PRX126 REF BOARD design enables the SFP module to be connected to an optical fiber. Ensure that the correct optical connector type, depending on the specific SFP module, is used. A fiber cable with an SC/APC connector must be used with the EASY PRX126 REF BOARD. SC/APC connectors typically have a green exterior.

3 Mode Settings

In the default EASY PRX126 REF BOARD operation mode, the boot mode $0xD_H$ is selected. Other boot modes are only selectable in conjunction with the EASY 98900 to update the uboot image in the case of a failure such as flash erase. Refer to [1] for more information on supported boot modes.

The default boot mode has these settings:

- QSPI Quad Bit NAND mode (the software is loaded from the NAND flash memory in the SFP Stick)
- Big-endian
- Boot flash at 1.8 V power rail
- JTAG Mode

This chapter describes special settings for the boot mode, the ASC, and the GPIO debug functions.

3.1 Boot Mode Settings

The PCB edge connector of the SFP module uses the MSA SFF-8419 standard [4]. This allows access to the boot mode signals.

To use the different boot modes, the three boot signals BOOT1, BOOT2, and BOOT3 of the PRX126 must be available via the external PCB connector. The EASY PRX126 REF BOARD uses one GND pin and the TxFAULT pins to access these signals. BOOT1 is connected to a GND pin, and BOOT2 and BOOT3 are connected to the Rate_Select pin because both signals must be at the same level and one signal is the UART0_TX. When use of different boot modes is not used or required, resistors must be soldered on to the PCB. Table 4 describes the configuration of these resistors.

Table 4 Optional Resistors for Mode Settings

Component	Setting	Function	Other Function
R42	Mounted (default)	NTR/TxFAULT signal is able to be used	Debug interface is able to be used (must be enabled by software)
	Not mounted	Tx_FAULT	-
R25	Not mounted (default)	NTR is not able to be used	-
	Mounted	NTR is able to be used when R42 is mounted	-
R35	Not mounted (default)	UART_RX is able to be used (see R41)	-
	Mounted	Dying Gasp feature is able to be used (R41 must not be mounted)	-
R41	Mounted (default)	UART_RX is connected to pin 7 of J1	-
	Not mounted	Dying Gasp feature is able to be used (see R35)	-
R28	Mounted (default)	UART_TX is connected to pin 2 of J1, all boot modes are able to be addressed where BOOT0 is '0'	-
	Not mounted	No UART_RX is able to be used, all QSPI boot modes are able to be selected	-

Table 4 Optional Resistors for Mode Settings (cont'd)

Component	Setting	Function	Other Function
R45	Mounted with 10 kΩ (default)	UART_RX in debug mode selected	-
	Mounted with 0 Ω	Only boot modes "Legacy UART" or "Quad SPI bit NAND" are able to be selected	-
R24	Not mounted (default)	Boot mode is able to be set externally via pin 2 of J1 (R33 and R42 must be mounted)	-
	Mounted	GPIO31 is set to '0', boot mode UART XMODEM or QSPI NOR is able to be selected	-
R33	Mounted (default)	Boot modes are able to be selected	-
	Not mounted	Boot mode must be set by R24	-
R22	Not mounted (default)	Tristate driver U2 must be mounted. TxFAULT is able to be connected to J1 via driver or disabled for UART_TX by software. GPIO30 is used as enable/disable signal for TxFAULT.	-
	Mounted	TxFAULT is used GPIO30 is used as TxFAULT (U2 removed)	-

Figure 5 shows the circuit diagram for the optional resistors and **Figure 6** shows their actual positions on the EASY PRX126 REF BOARD.

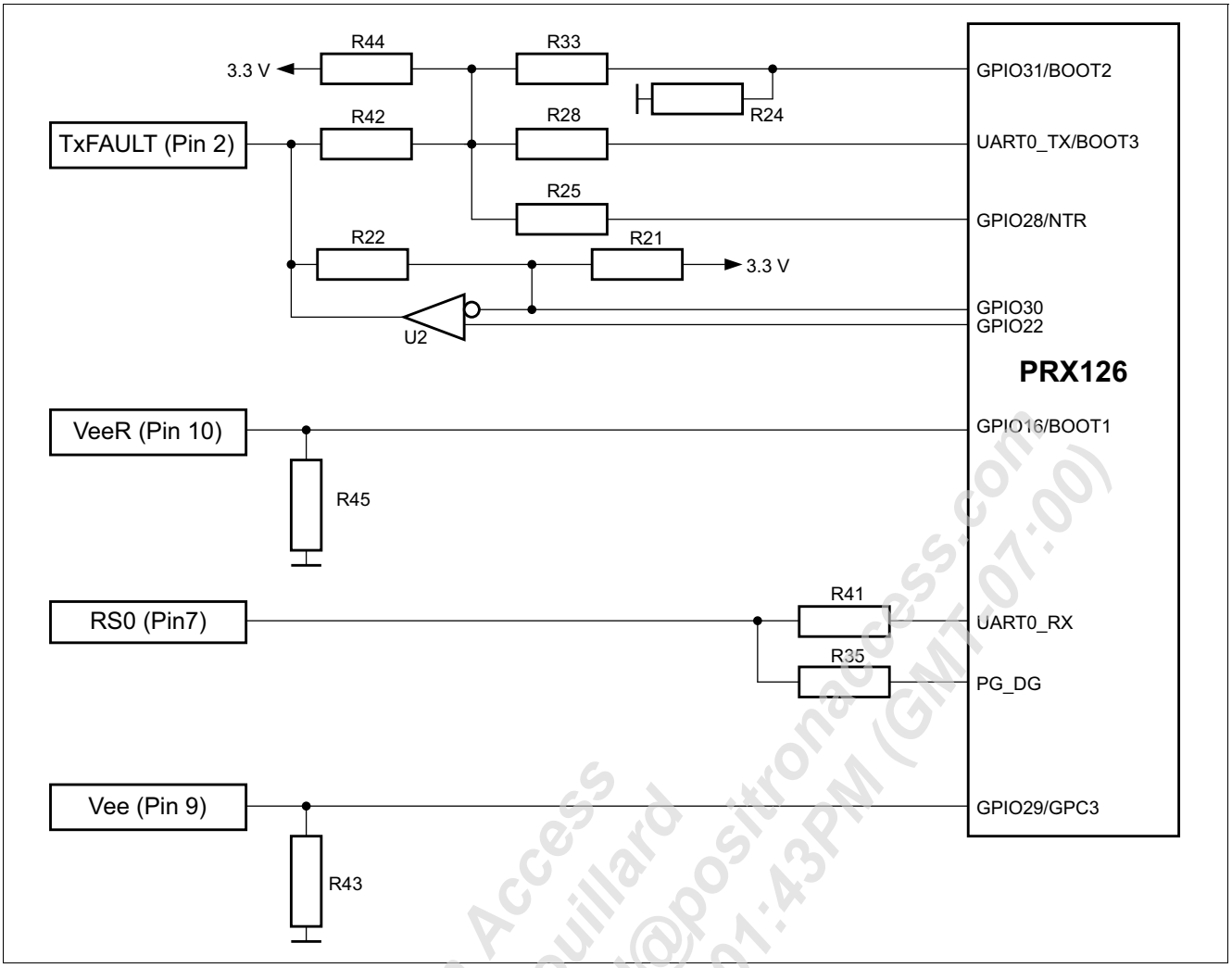

Figure 5 Circuit Diagram Showing Optional Resistors on the EASY PRX126 REF BOARD

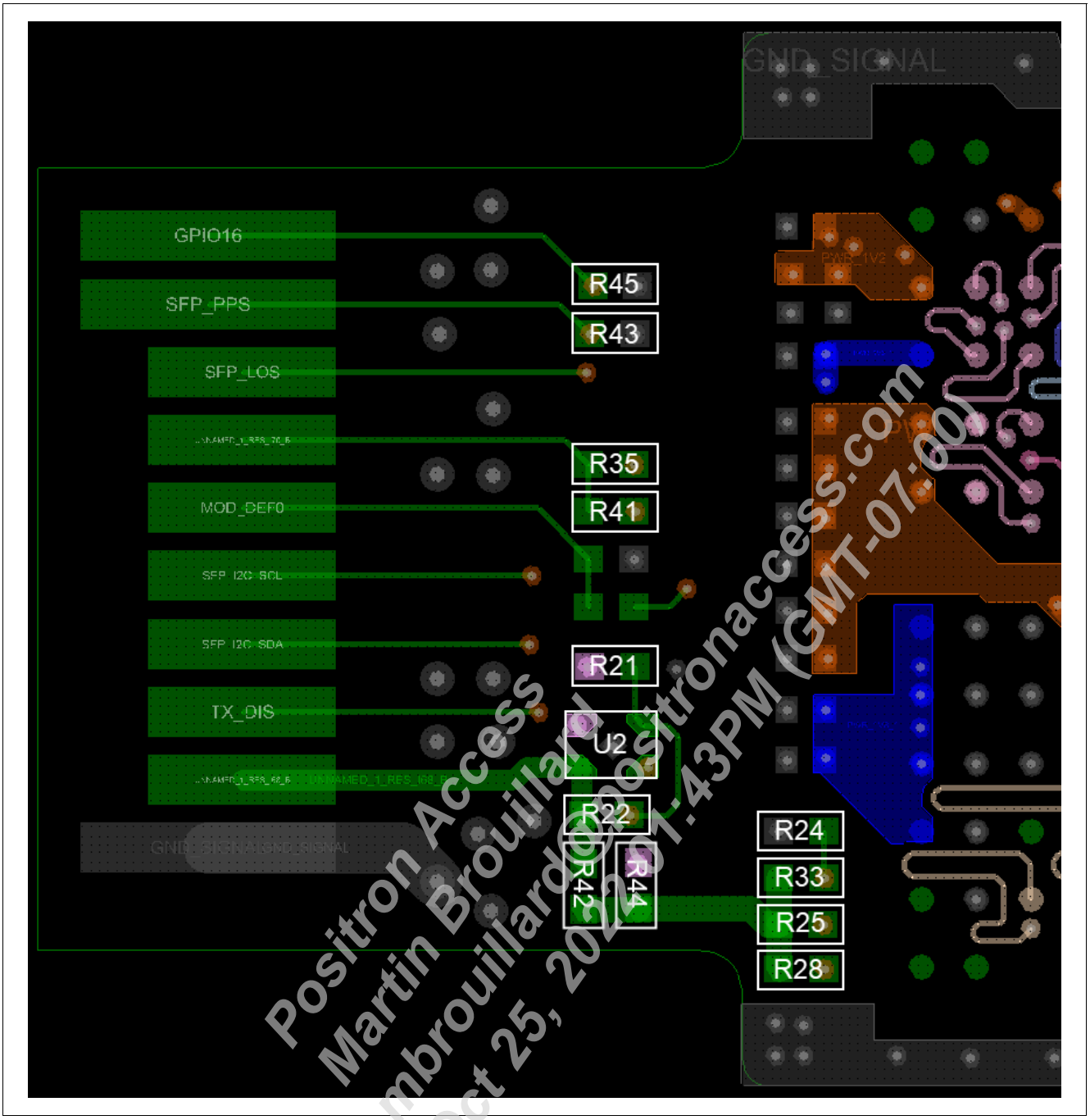

Figure 6 Positions of Optional Resistors on the EASY PRX126 REF BOARD

3.2 Asynchronous Serial Interface (ASC)

The RS-232 interface uses low voltage levels and the signals UART0_RX and UART0_TX. This interface is not normally available on the connector, but UART0_RX and UART0_TX are connected to the edge connector and are used as standard GPIOs for Rate_Select (UART0_RX) and Tx_Fault (UART0_TX). Therefore, both interface signals are selected via hardware for use as either standard GPIOs or as a debug interface.

The ASC interface is only used during the development phase to download software or provide access to internal registers for debugging purposes. There is one method for the initial downloading of software to the EASY PRX126 REF BOARD:

- Via the RS-232 interface

The EASY PRX126 REF BOARD is configurable to allow the ASC interface of the EASY 98900 to be accessed via the edge connector. The signals TxFAULT and Rate_Select use GPIOs of the EASY 98900 that are also usable as an ASC interface. This is configured via software, as described in [2]. No hardware selection or other setting is necessary to use the debug interface, however the system that is used with the EASY PRX126 REF BOARD must support the feature.

The TX_FAULT signal is configurable to provide one of these functions:

- TxFAULT (as module present)
- UART0_TX
- NTR

Rate_Select is an input signal and is used as the second signal of the debug interface:

- DY_GASP
- UART0_RX

3.3 GPIO Debug Function Mode

Refer to [3] for more details on the configuration register options that allow switching between standard GPIO functionality and the special debug functions.

4 EASY PRX126 REF BOARD Dimension Drawing

Figure 7 shows a top view drawing of the EASY PRX126 REF BOARD, including dimensions.

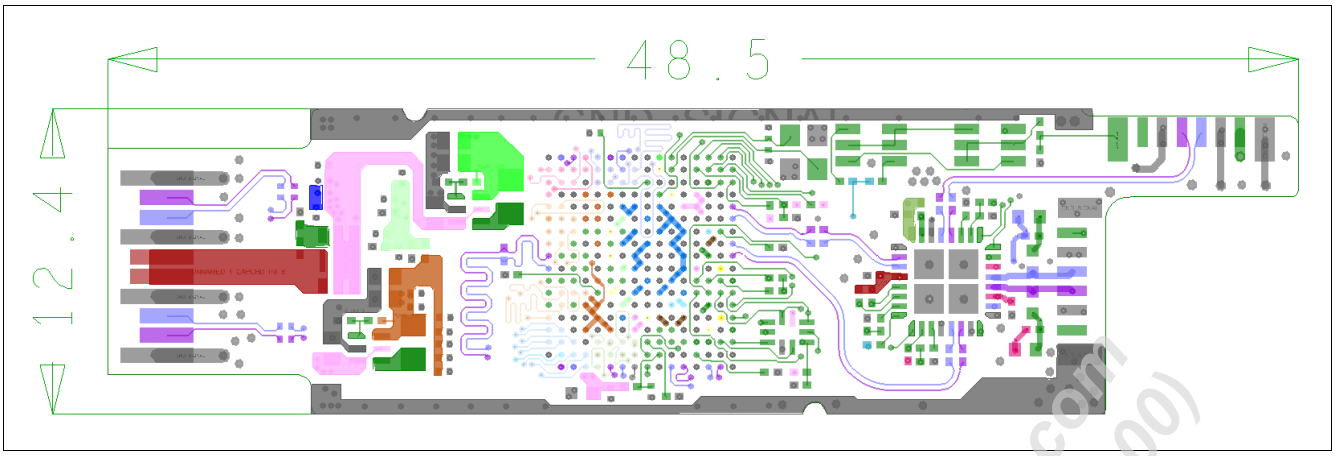

Figure 7 EASY PRX126 REF BOARD Dimension Drawing

Literature References

[1] 10G PON Chipset PRX126 (PRX126B0BI/PRX126B1BI/PRX126B2BI) Data Sheet Rev. 3.4

[2] 10G PON Chipset System Overview Rev. 3.0

[3] 10G PON Subsystem Programmer's Guide Rev. 2.2

Attention: Refer to the latest revisions of the documents.

Standards References

[4] SFF-8419, SFP+ Power and Low Speed Interface
https://www.snia.org/technology-communities/sff/specifications

Terminology

A	
APD	Avalanche Photodiode
ASC	Asynchronous Serial Interface
B	
BOSA	Bi-directional Optical Sub Assembly
L	
LDO	Low Dropout
LOS	Loss of Signal
M	
MSA	Multi-Source Agreement Group
O	
ONT	Optical Network Termination
P	
PCB	Printed Circuit Board
PMD	Physical Media Dependent
PPS	Pulses per Second
S	
SDRAM	Synchronous Dynamic Random Access Memory
SFP	Small Form-Factor Pluggable
SGMII	Serial Gigabit Media-Independent Interface
SPI	Serial Peripheral Interface
T	
ToD	Time-of-Day